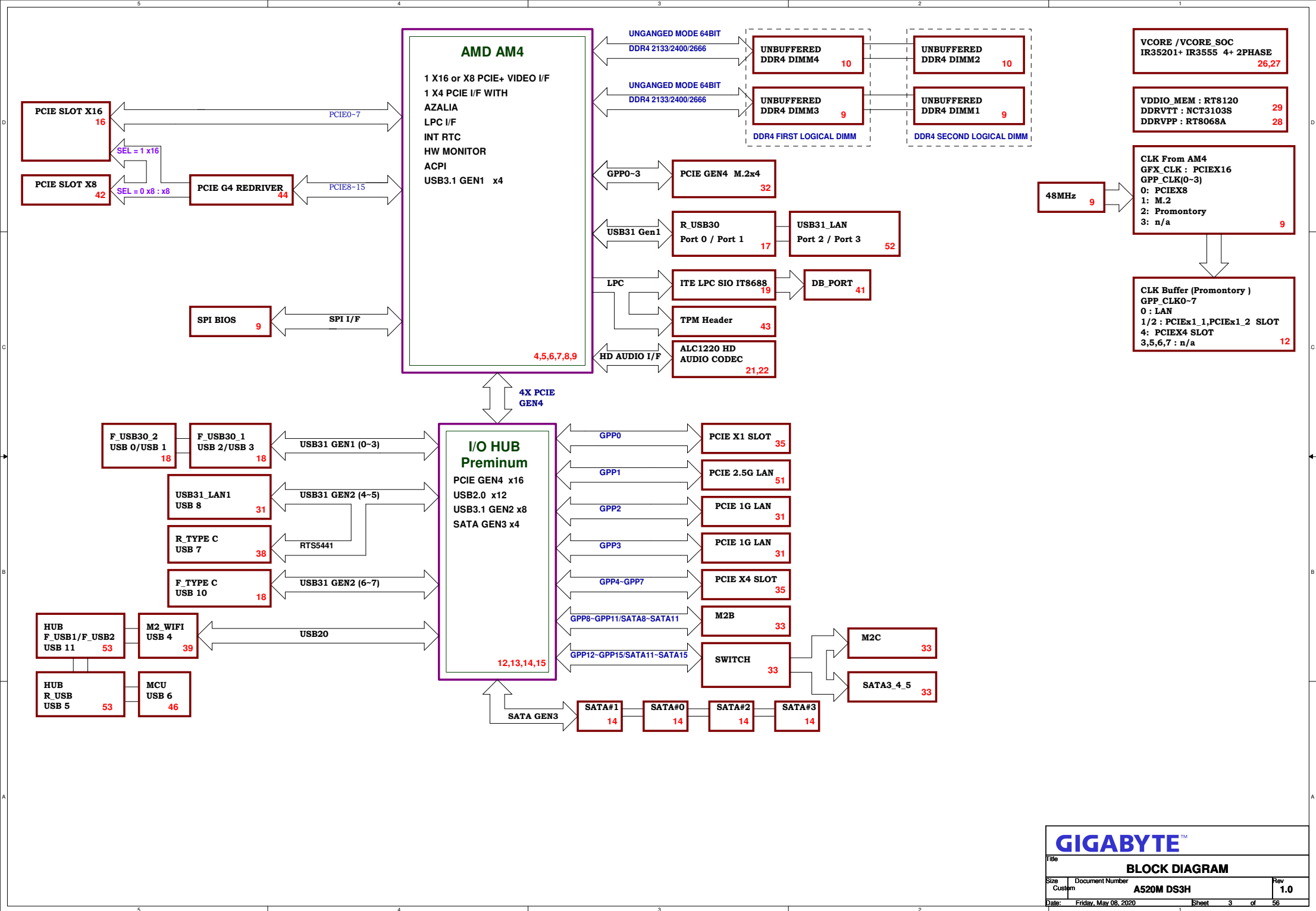
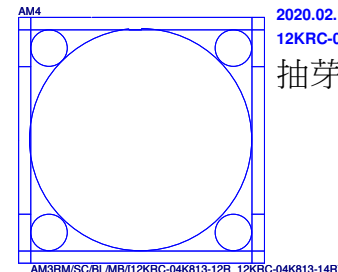
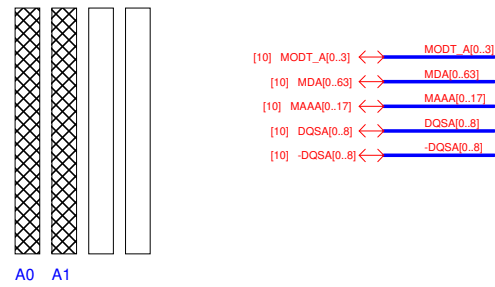


A520M DS3H

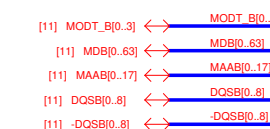
PAGE	TITLE	Revision : 1.0
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU DDR4 MEMORY	
05	CPU CONTROL	
06	CPU GFX, GPP, SB, GND	
07	CPU ACPI/GPIO/USB/AUDIO	
08	CPU POWER & GND	
09	CPU CLK/SPI/USB	
10	DDR4 CHANNEL A	
11	DDR4 CHANNEL B	
12	PM CLK/GPIO/FAN	
13	PM USB	
14	PM UMI/GPP/SATA	
15	PM POWER & GND	
16	PCI EXPRESS x16	
17	PCI EXPRESS x4 / x1	
18	IT8688	
19	FAN. HWM, TPM	
20	PWM RAA229004	
21	VCORE MOS1	
22	VCORE MOS2	
29	POWER SEQ, A_VDDP	
30	DDR POWER , 5VDUAL	
31	VPPMEM, OC DAC	



MEM CHA



2020.02.17
12KRC-04K813-12R/14R
抽芽式



GIGABYTE™

Title: **APU DDR4**

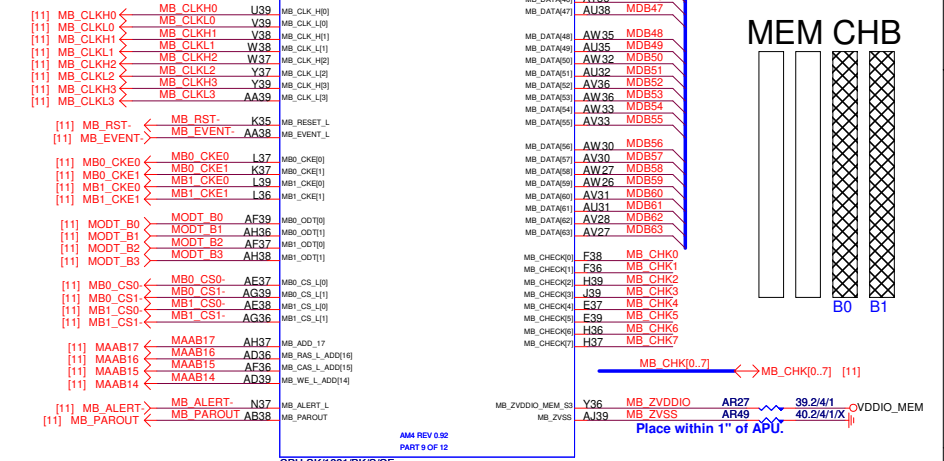
Size: Custom Document Number: **A520M DS3H** Rev: **1.0**

Date: Tuesday, May 19, 2020 Sheet: 4 of 56

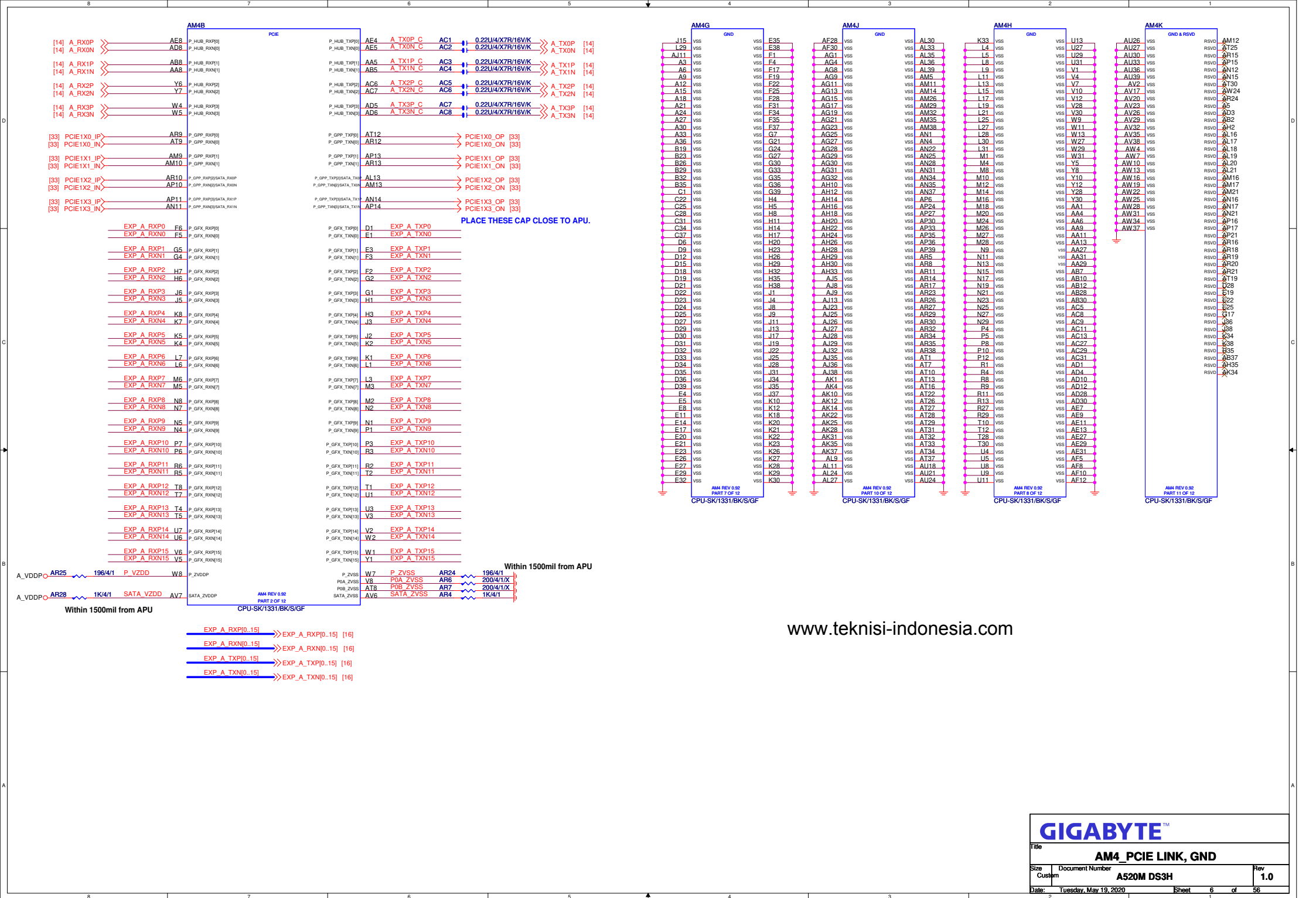
A0 A1

B0 B1

MEM CHB

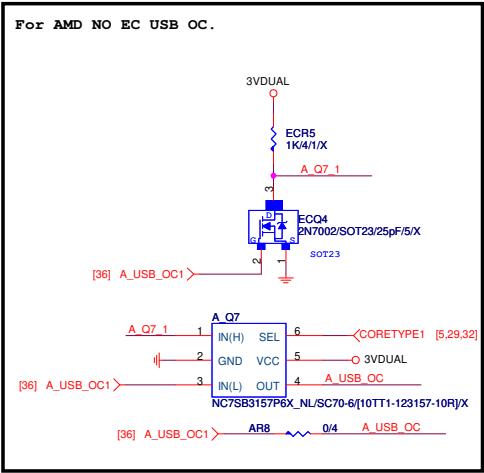
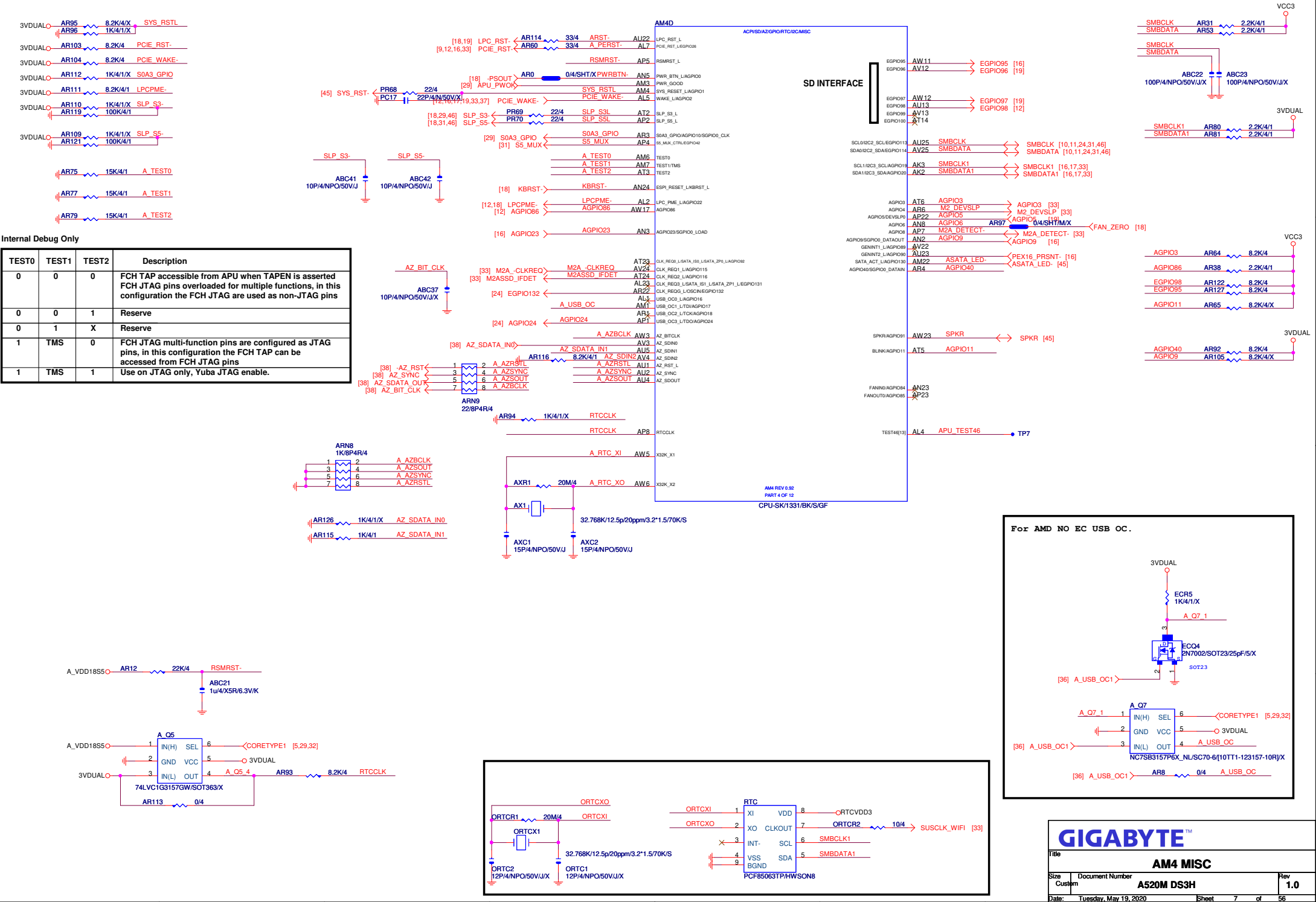


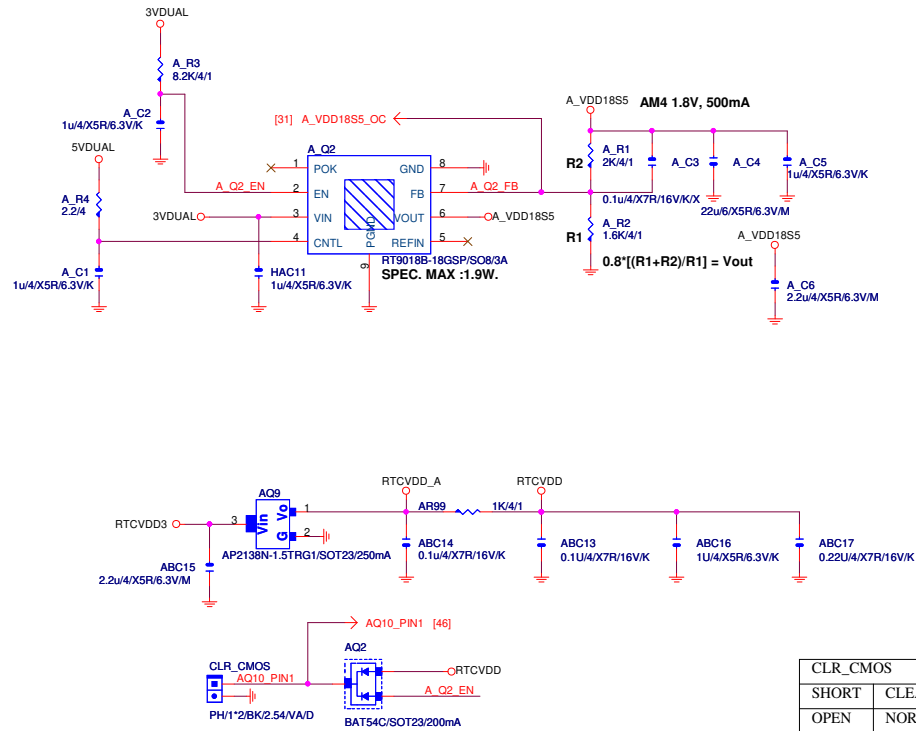
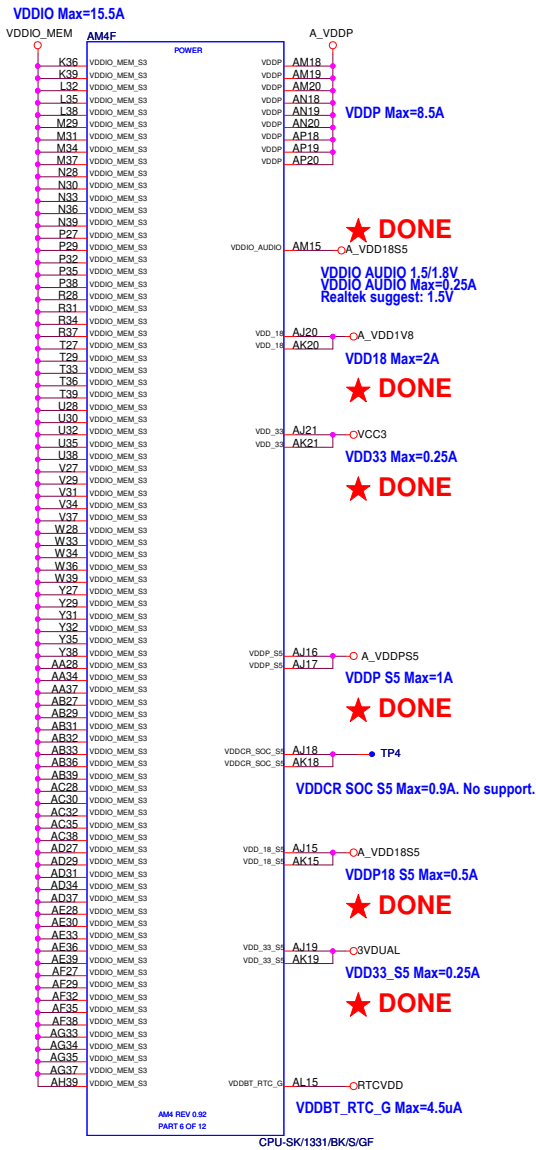
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CPU CONTROL			
Size	Document Number	Rev	
Custom	A520M DS3H	1.0	
Date:	Tuesday, May 19, 2020	Sheet	5 of 56



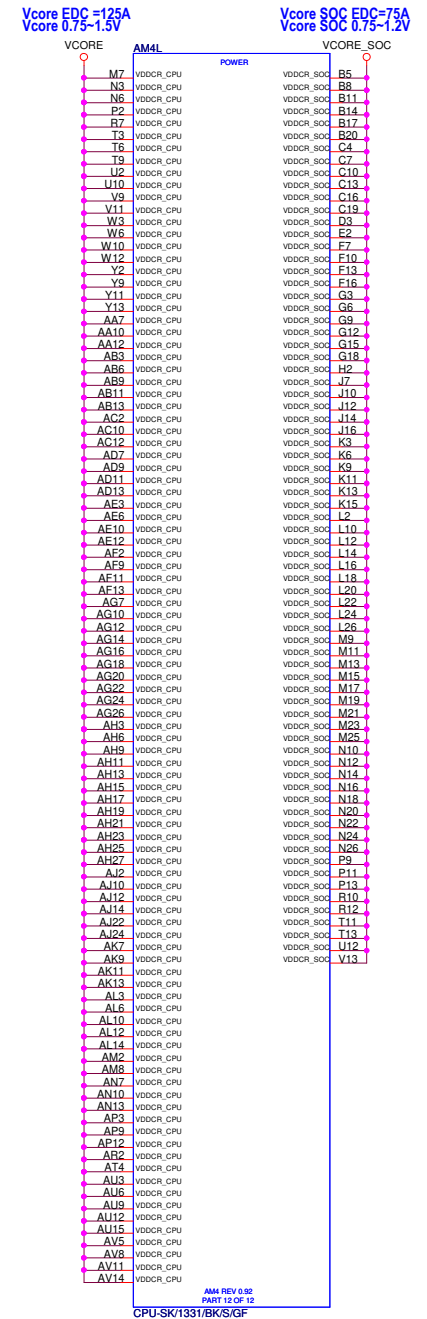
Internal Debug Only

TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.

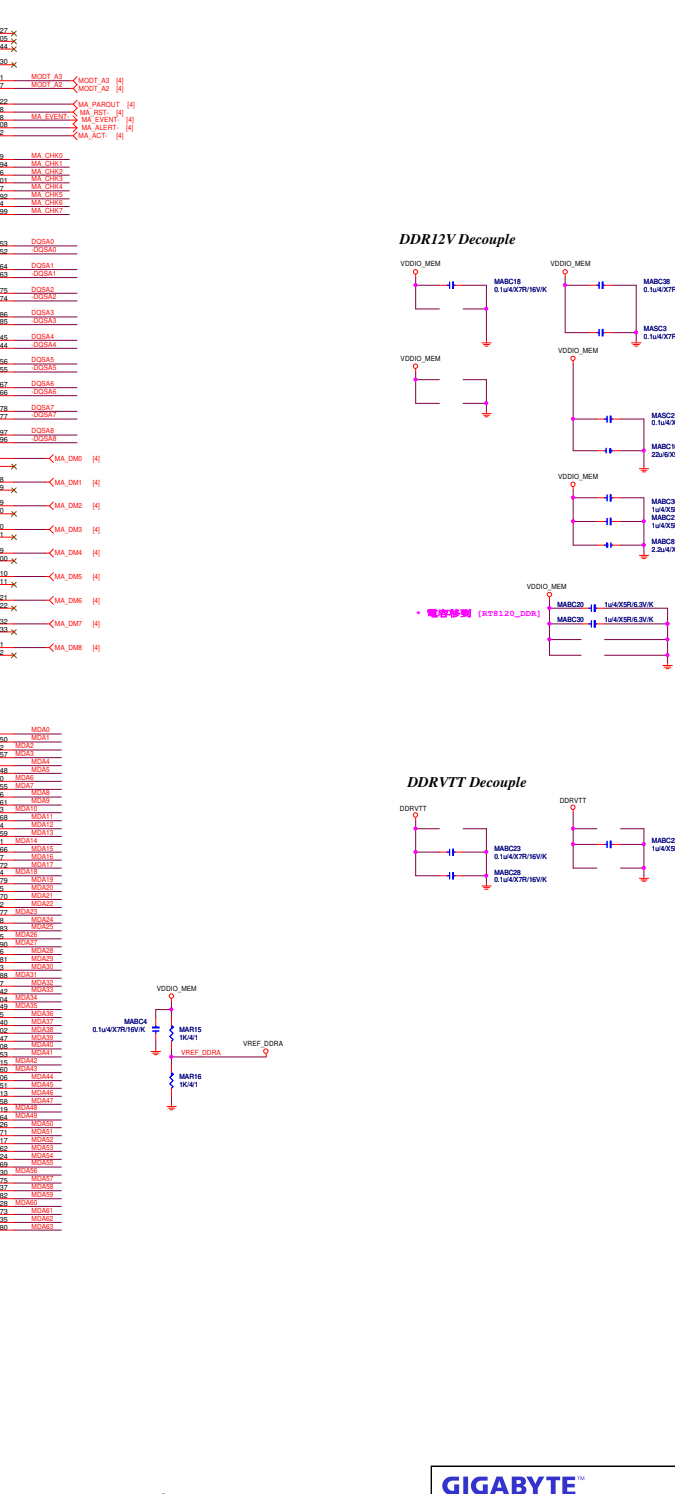
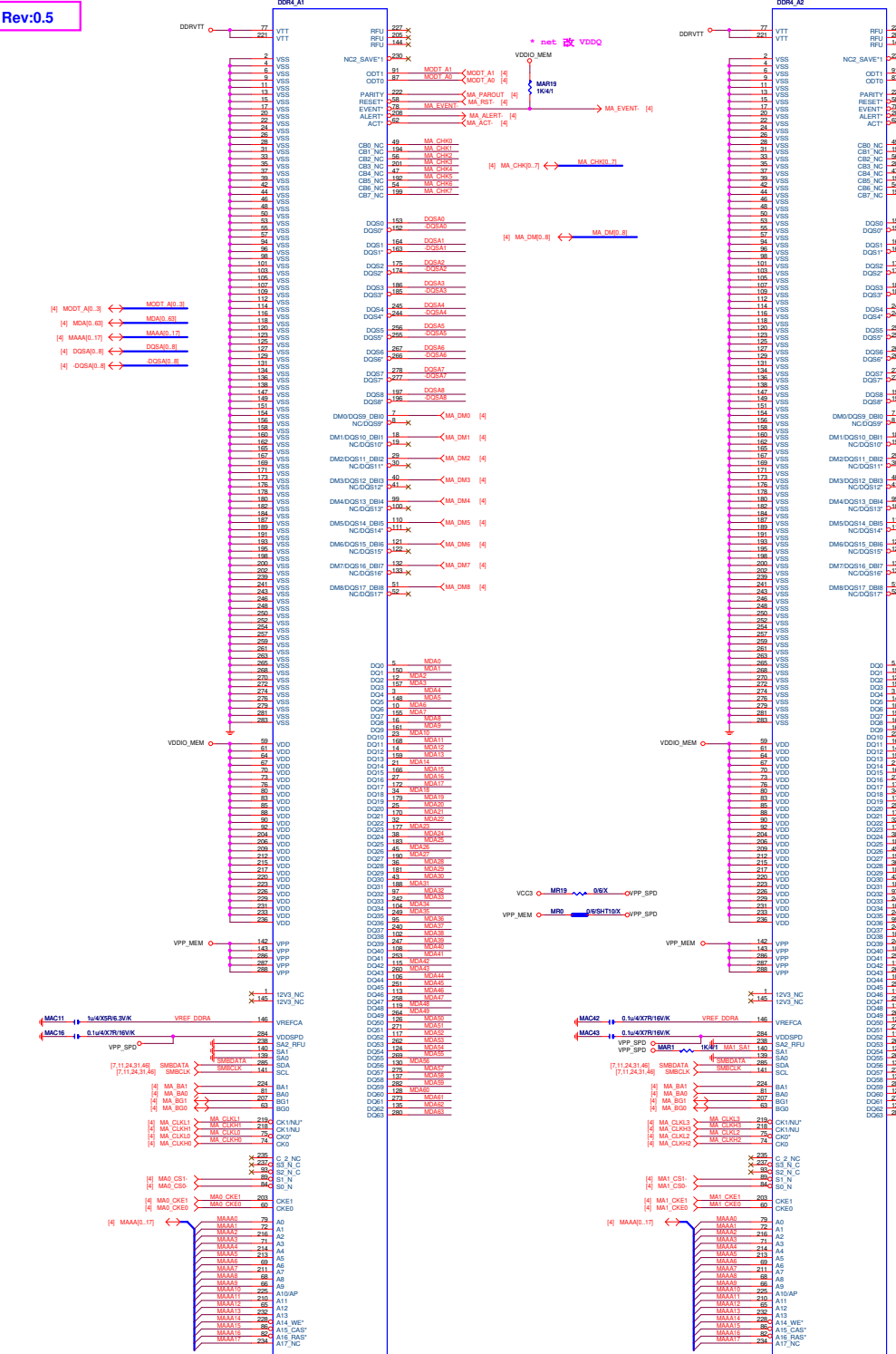




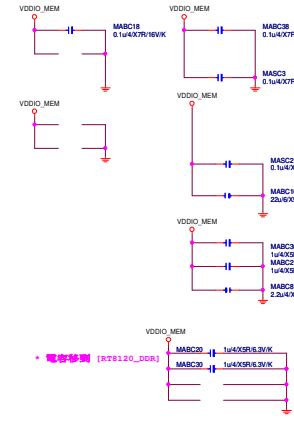
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL
NOT ADD ICT FOR RTCVDD PIN	



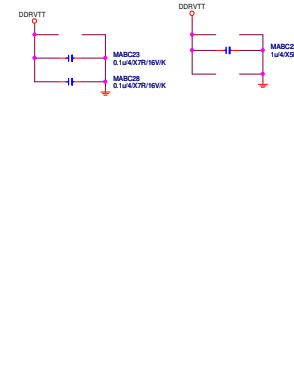
GIGABYTE™			
Title CPU POWER & GND			
Size Custom	Document Number A520M DS3H	Rev 1.0	
Date: Tuesday, May 19, 2020	Sheet 8	of 56	



DDR12V Decouple



DDRVRTT Decouple

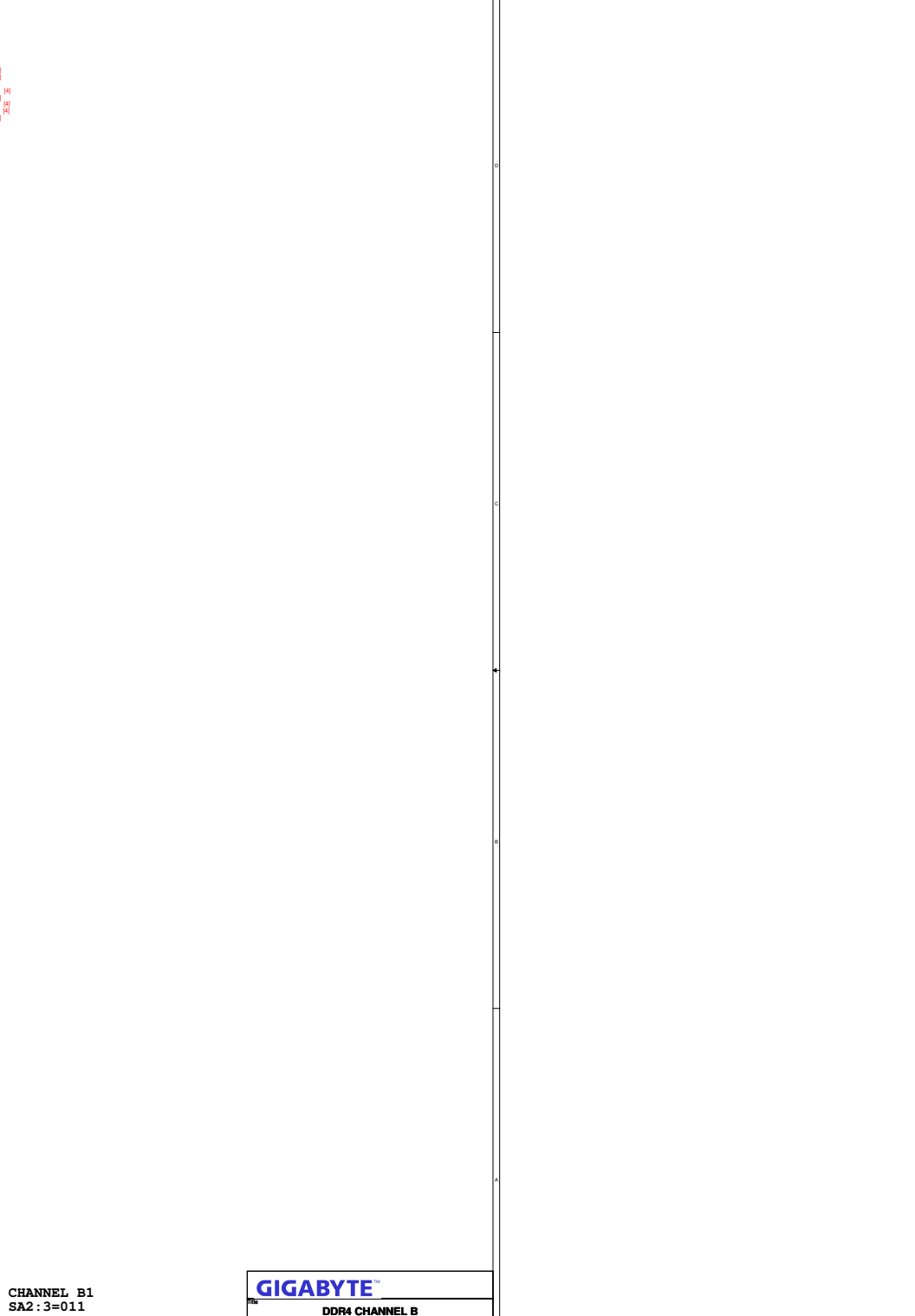


CHANNEL A0
SA2:0=000

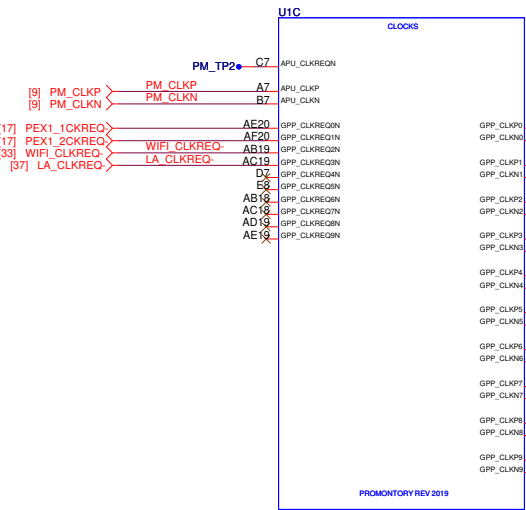
CHANNEL A1
SA2:2=010



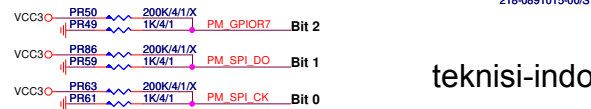
CHANNEL B0
SA2:1=001



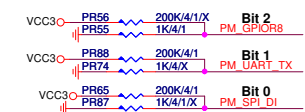
CHANNEL B1
SA2:3=011



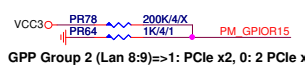
R0.2 Update
CLK & CLK REQ 需與PCIE Port mapping



Bit 2	Bit 1	Bit 0	GPP Group 0 (Lanes 3:0)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
Others: Reserved			

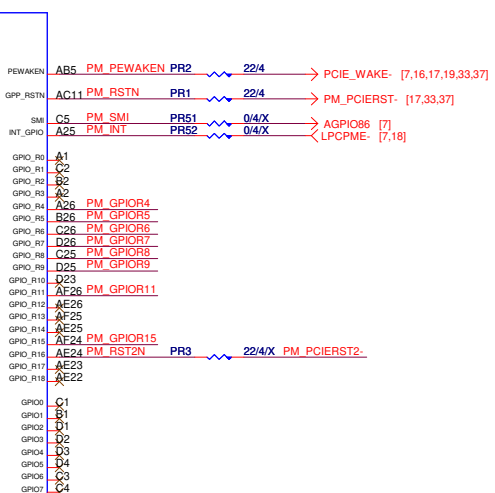
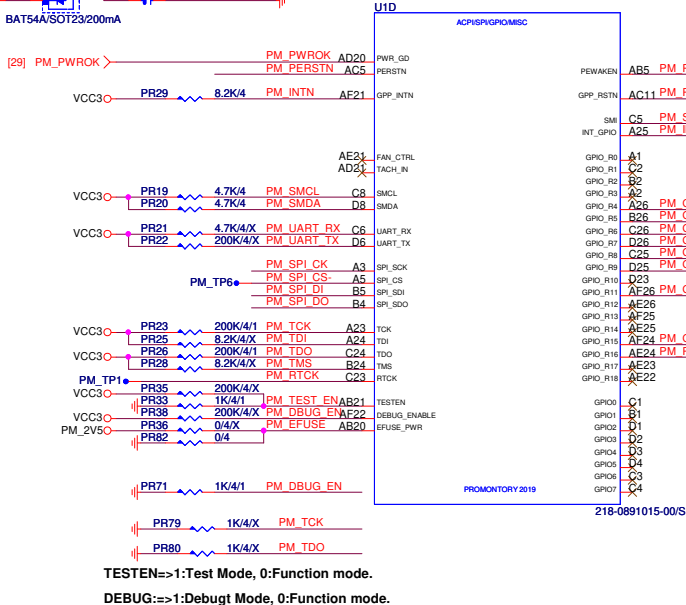
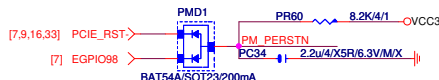


Bit 2	Bit 1	Bit 0	GPP Group 1 (Lanes 7:4)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
Others: Reserved			

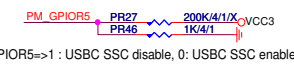


GPP Group 2 (Lan 8:9)=>1: PCIe x2, 0: 2 PCIe x1

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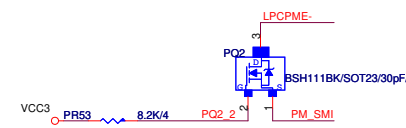
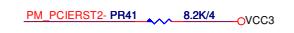
GPIOR4 1: GPP clock source from APU_CLKP/N;
0: GPP clock source from Crystal.



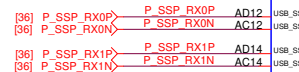
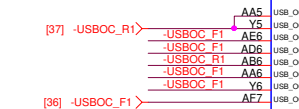
GPIOR5=>1: USB SSC disable, 0: USB SSC enable



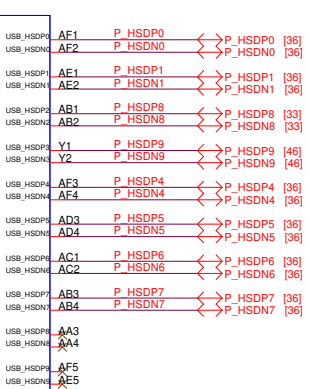
GPIOR6=>1: SATA SSC disable, 0: SATA SSC enable



USB port power control 9:0
(VCC3). Output.



USB32G2	USB20	USB_OC
0	0	0
1	1	1
USB32G1		
0	2	2
1	3	3
	4	4
	5	5
	6	6
	7	7
	8	7
	9	7



USB 3.1 Gen 1

HSD 2

HSD 3

USB 3.1 Gen 2

HSD 0 F_USB30 OK

HSD 1 F_USB30 OK

F_USB30 OK

F_USB30 OK

M2 WIFI OK

MCU OK

KB_MS_USB OK

KB_MS_USB OK

F_USB20 OK

F_USB20 OK

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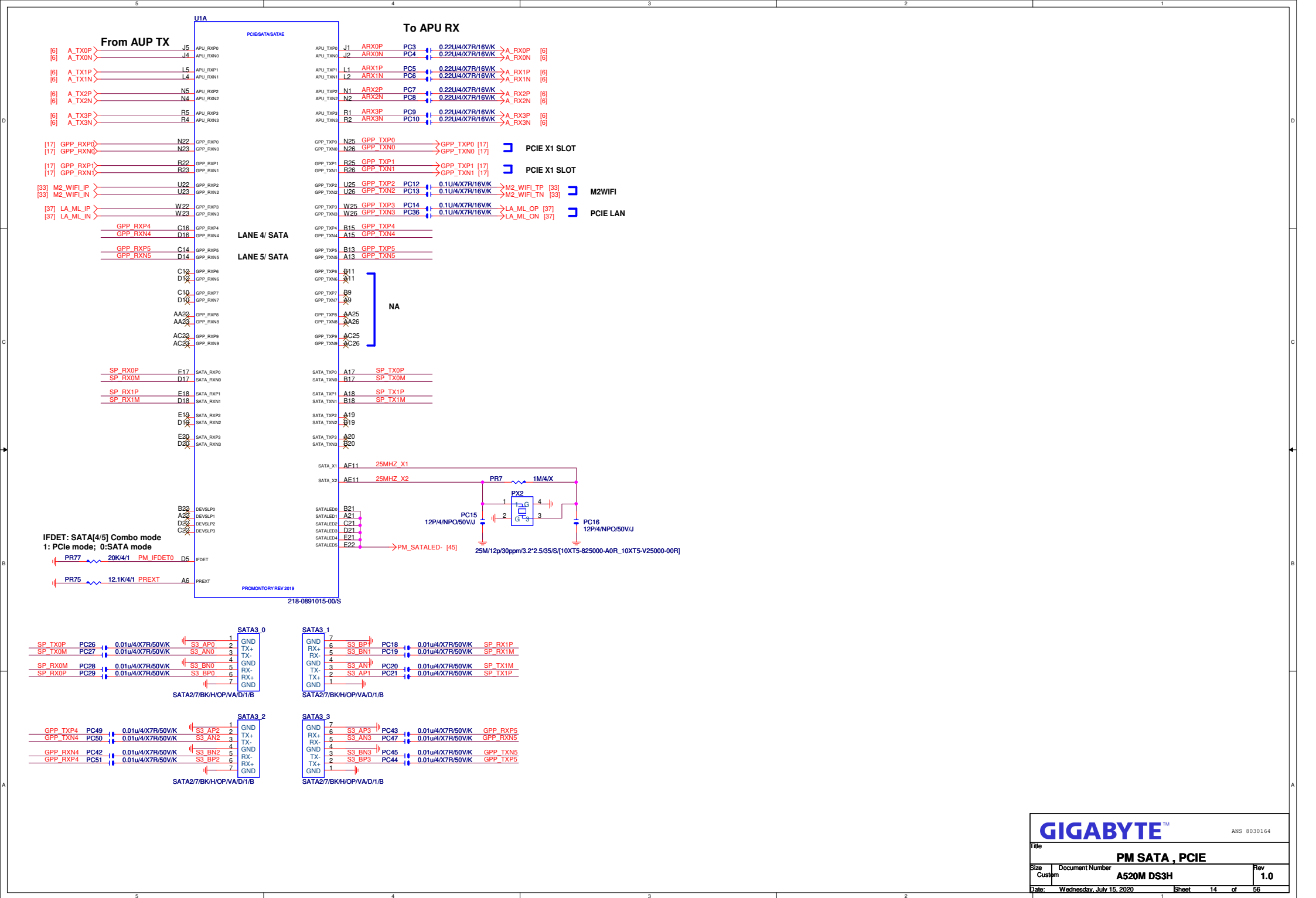
ANS 8030164

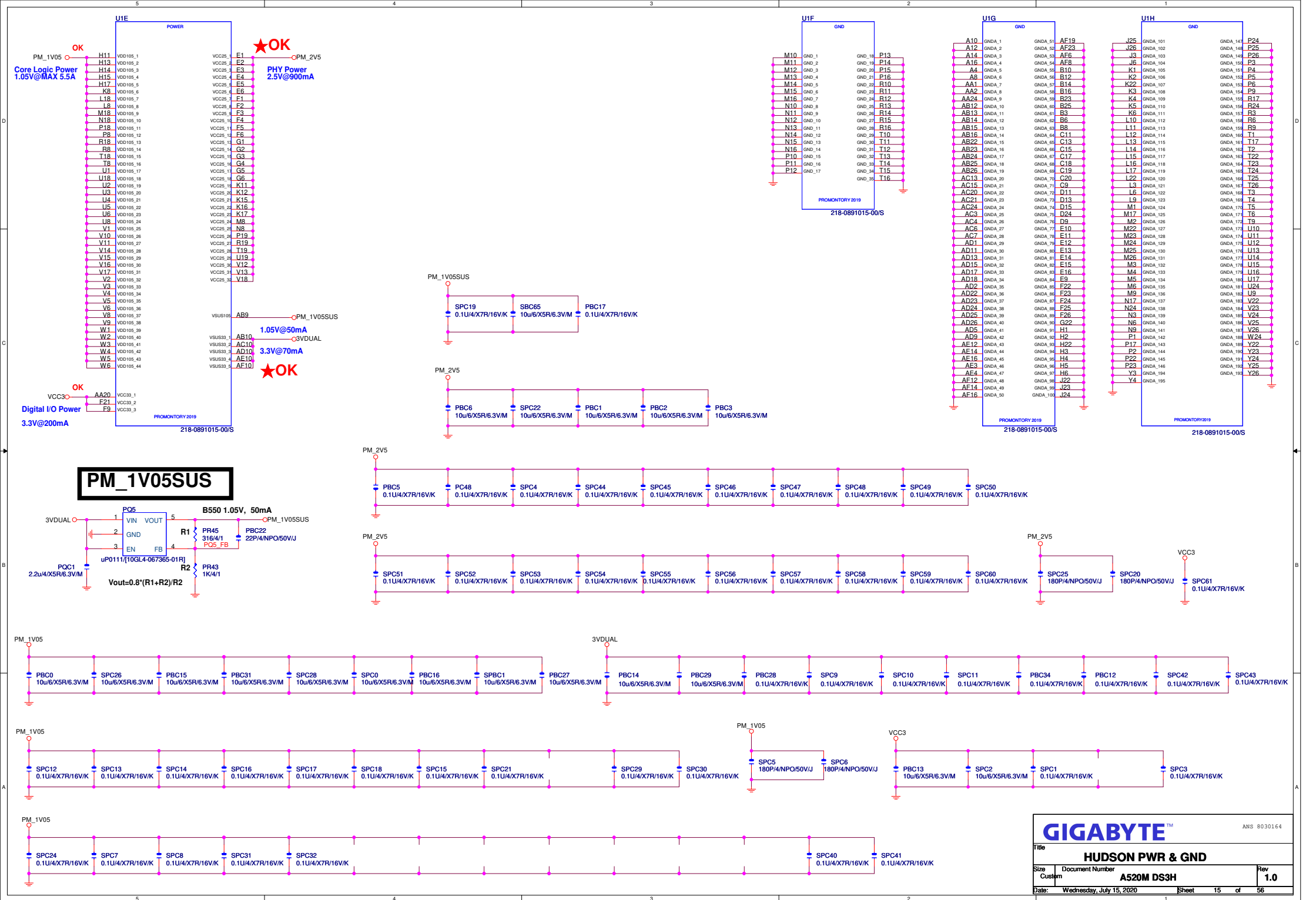
Title PM USB

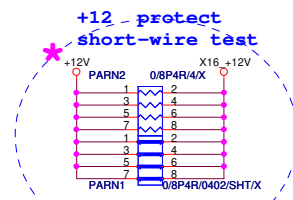
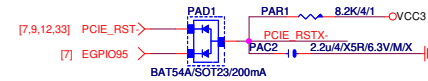
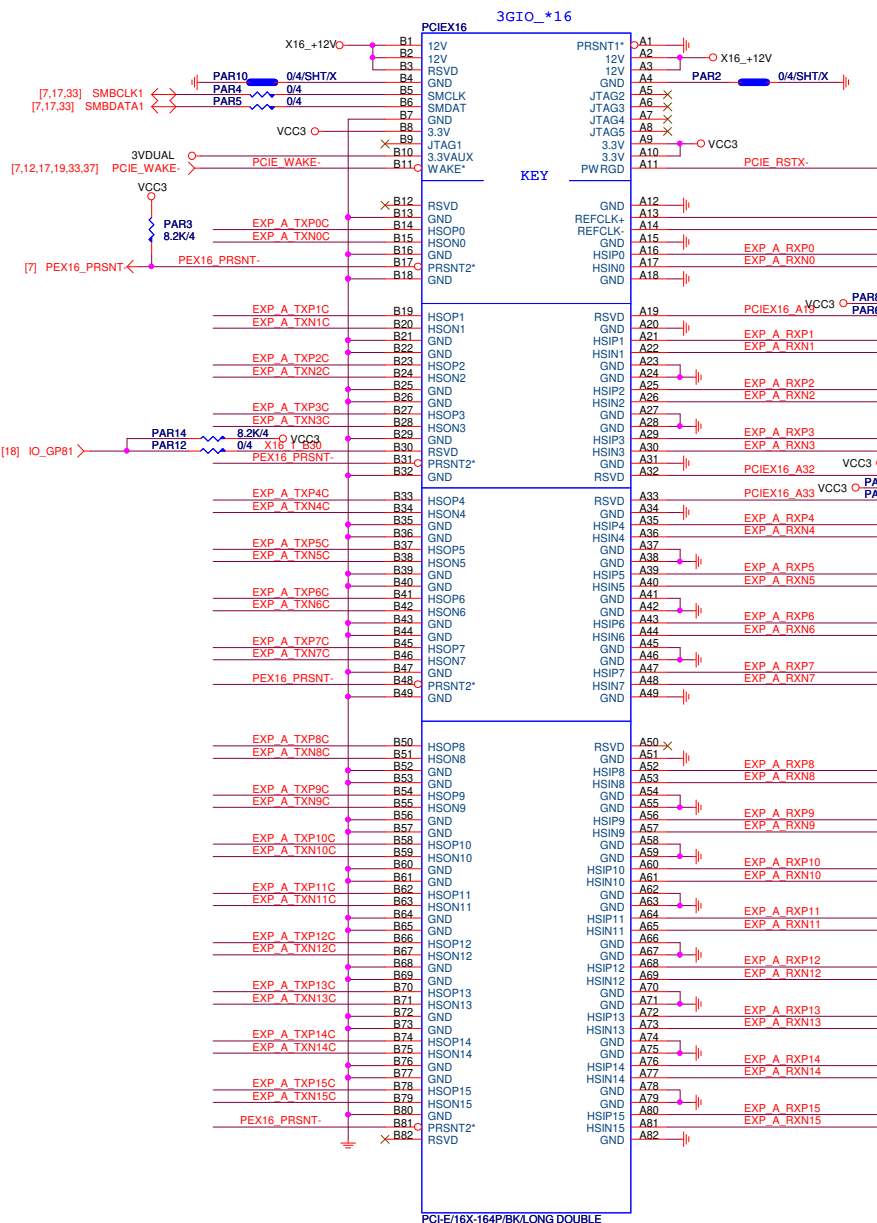
Size Custom Document Number A520M DS3H

Rev 1.0

Date: Wednesday, July 15, 2020 Sheet 13 of 56



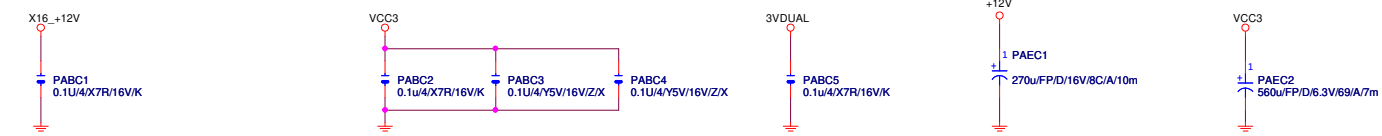


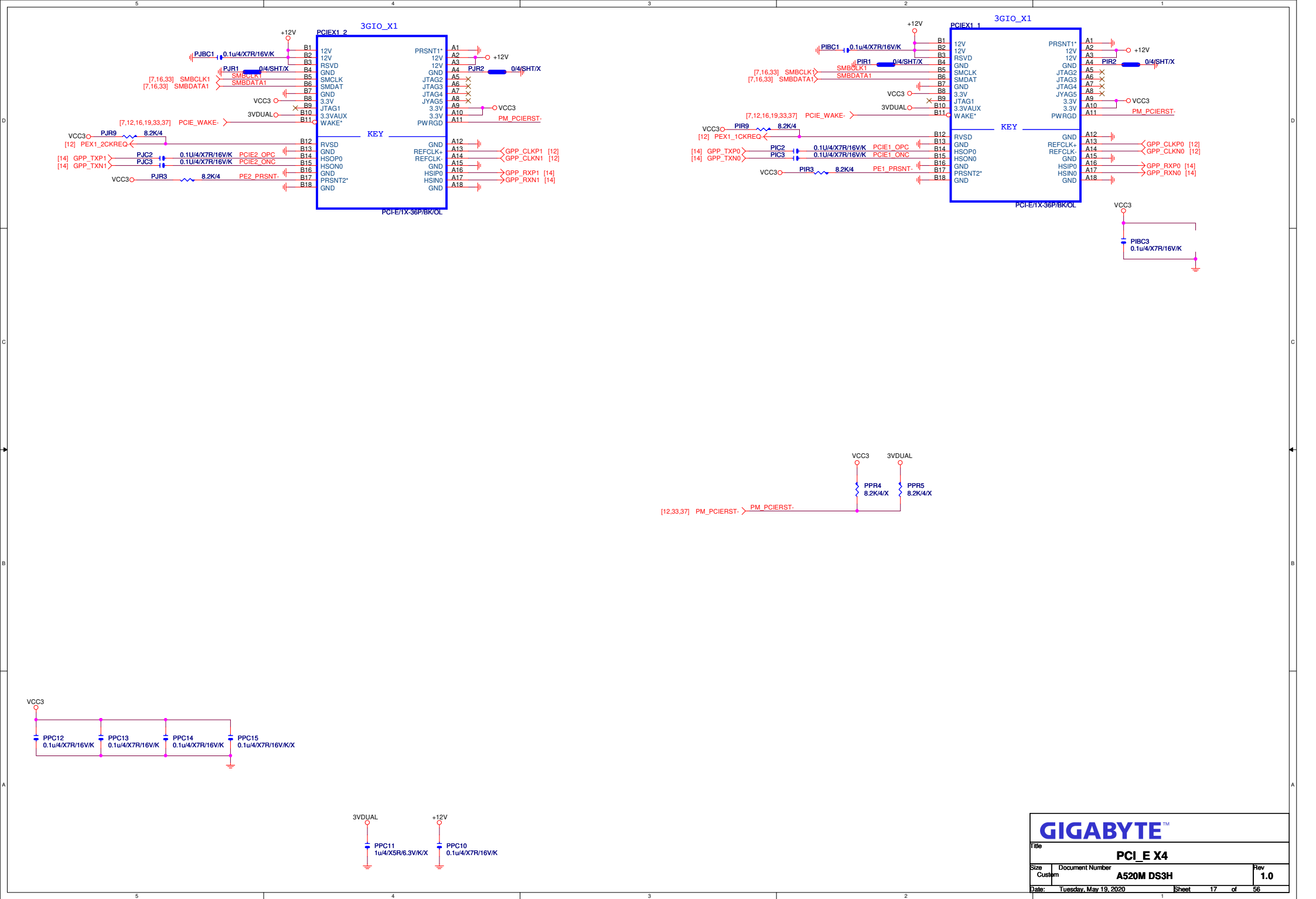


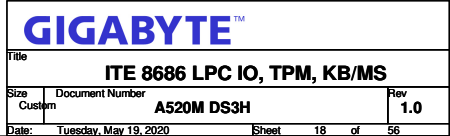
EXP A TXP0	PAC4	0.22u/4X5R6.3V/K	EXP A TXP0C
EXP A TXN0	PAC5	0.22u/4X5R6.3V/K	EXP A TXN0C
EXP A TXP1	PAC6	0.22u/4X5R6.3V/K	EXP A TXP1C
EXP A TXN1	PAC7	0.22u/4X5R6.3V/K	EXP A TXN1C
EXP A TXP2	PAC8	0.22u/4X5R6.3V/K	EXP A TXP2C
EXP A TXN2	PAC9	0.22u/4X5R6.3V/K	EXP A TXN2C
EXP A TXP3	PAC10	0.22u/4X5R6.3V/K	EXP A TXP3C
EXP A TXN3	PAC11	0.22u/4X5R6.3V/K	EXP A TXN3C
EXP A TXP4	PAC12	0.22u/4X5R6.3V/K	EXP A TXP4C
EXP A TXN4	PAC13	0.22u/4X5R6.3V/K	EXP A TXN4C
EXP A TXP5	PAC14	0.22u/4X5R6.3V/K	EXP A TXP5C
EXP A TXN5	PAC15	0.22u/4X5R6.3V/K	EXP A TXN5C
EXP A TXP6	PAC16	0.22u/4X5R6.3V/K	EXP A TXP6C
EXP A TXN6	PAC17	0.22u/4X5R6.3V/K	EXP A TXN6C
EXP A TXP7	PAC18	0.22u/4X5R6.3V/K	EXP A TXP7C
EXP A TXN7	PAC19	0.22u/4X5R6.3V/K	EXP A TXN7C
EXP A TXP8	PAC20	0.22u/4X5R6.3V/K	EXP A TXP8C
EXP A TXN8	PAC21	0.22u/4X5R6.3V/K	EXP A TXN8C
EXP A TXP9	PAC22	0.22u/4X5R6.3V/K	EXP A TXP9C
EXP A TXN9	PAC23	0.22u/4X5R6.3V/K	EXP A TXN9C
EXP A TXP10	PAC24	0.22u/4X5R6.3V/K	EXP A TXP10C
EXP A TXN10	PAC25	0.22u/4X5R6.3V/K	EXP A TXN10C
EXP A TXP11	PAC26	0.22u/4X5R6.3V/K	EXP A TXP11C
EXP A TXN11	PAC27	0.22u/4X5R6.3V/K	EXP A TXN11C
EXP A TXP12	PAC28	0.22u/4X5R6.3V/K	EXP A TXP12C
EXP A TXN12	PAC29	0.22u/4X5R6.3V/K	EXP A TXN12C
EXP A TXP13	PAC30	0.22u/4X5R6.3V/K	EXP A TXP13C
EXP A TXN13	PAC31	0.22u/4X5R6.3V/K	EXP A TXN13C
EXP A TXP14	PAC32	0.22u/4X5R6.3V/K	EXP A TXP14C
EXP A TXN14	PAC33	0.22u/4X5R6.3V/K	EXP A TXN14C
EXP A TXP15	PAC34	0.22u/4X5R6.3V/K	EXP A TXP15C
EXP A TXN15	PAC35	0.22u/4X5R6.3V/K	EXP A TXN15C

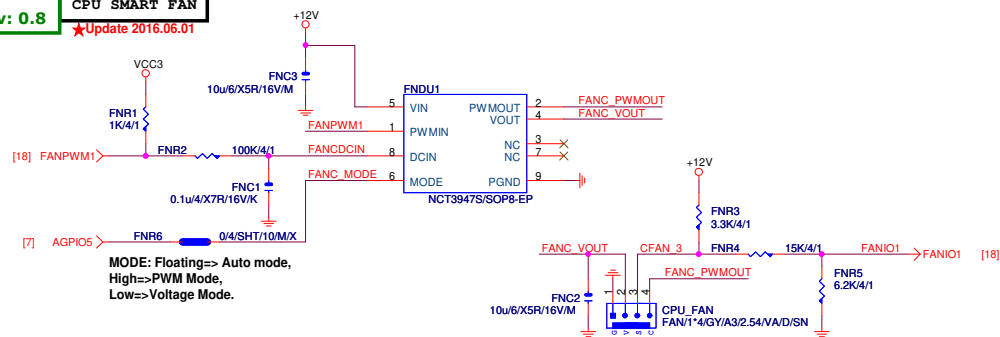
EXP A RXP[0..15] >>> EXP_A_RXP[0..15] [6]
 EXP A RXN[0..15] >>> EXP_A_RXN[0..15] [6]
 EXP A TXP[0..15] >>> EXP_A_TXP[0..15] [6]
 EXP A TXN[0..15] >>> EXP_A_TXN[0..15] [6]

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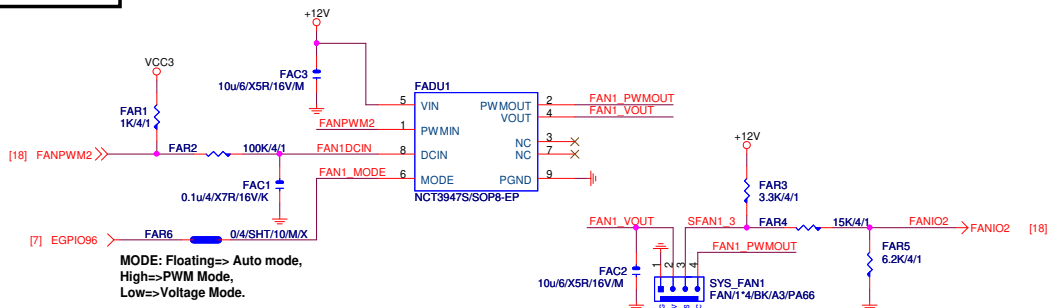




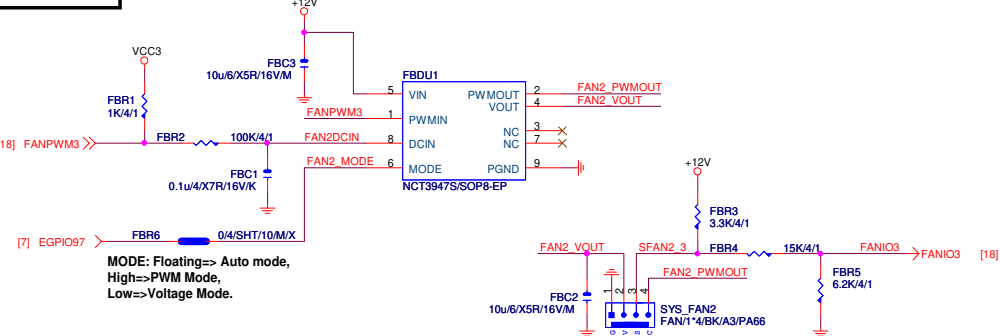




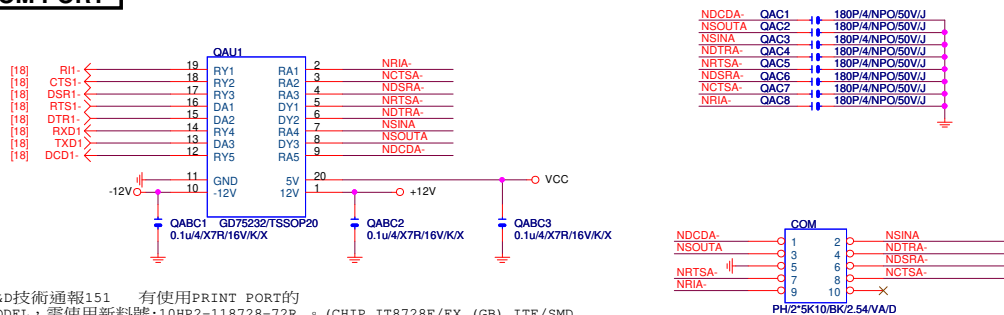
SYSTEM FAN1



SYSTEM FAN2

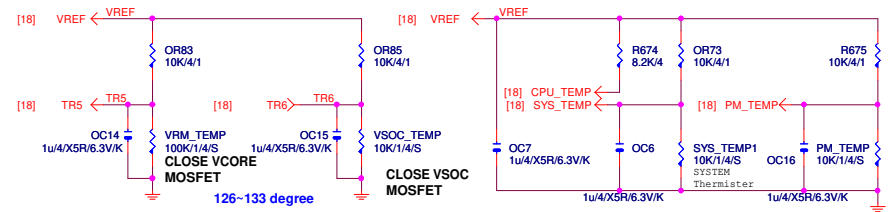


COM PORT

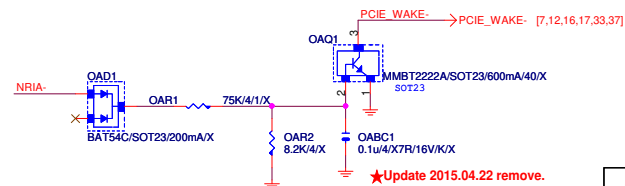
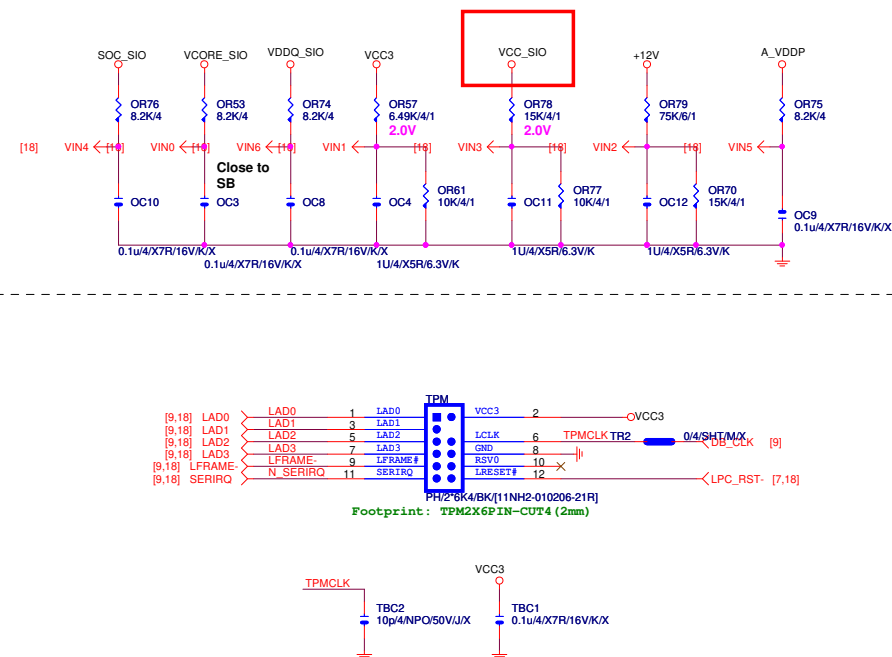


R&D技術通報151 有使用PRINT PORT的
MODEL, 需使用新料號:10HP2-118728-72R。(CHIP IT8728F/EX (GB) ITE/SMD
QFP128 PRINTPORT SORTING)料件。串電阻33 ohm改為68 ohm。

Hardware Monitor circuits - Temperature

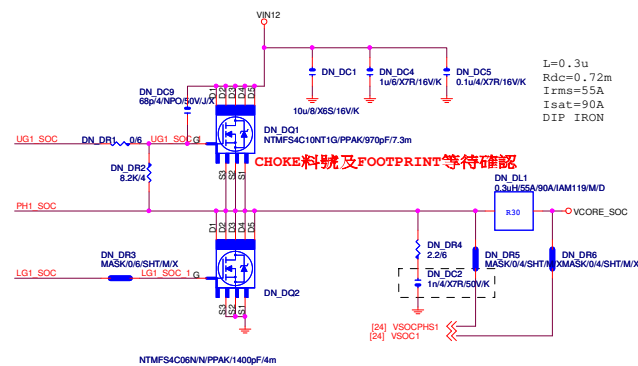
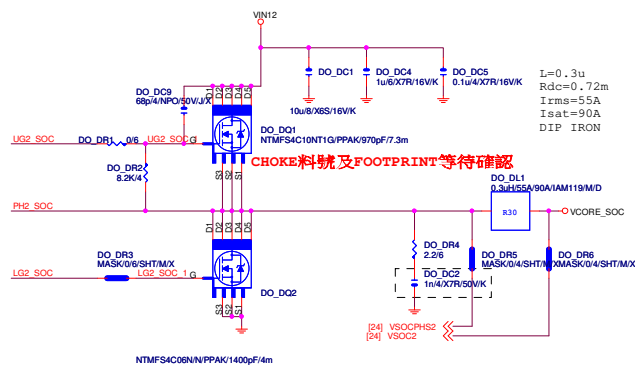
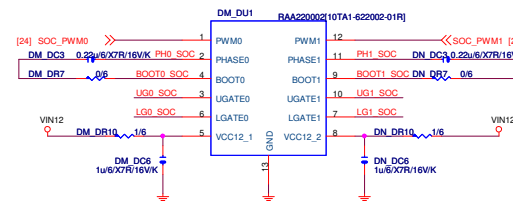
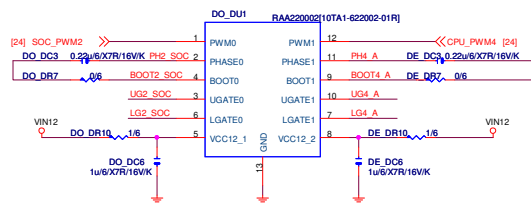
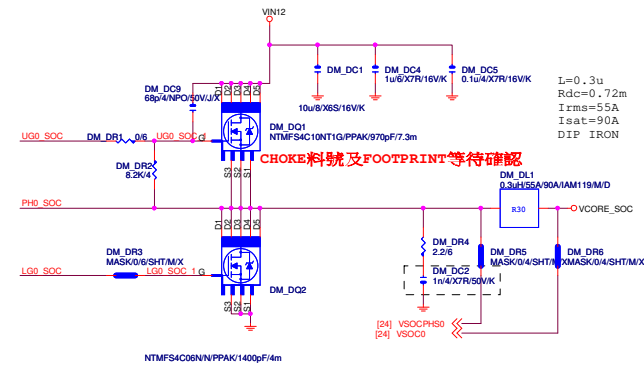
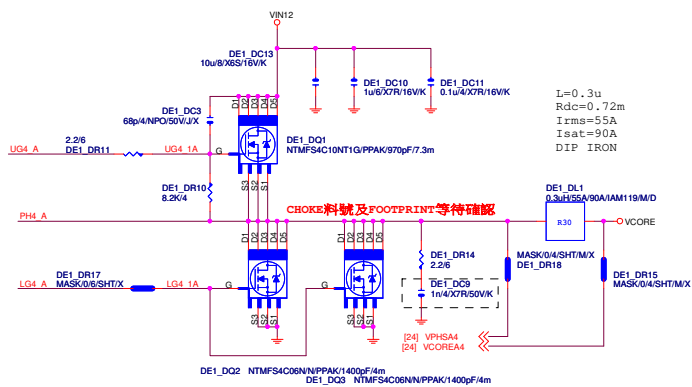


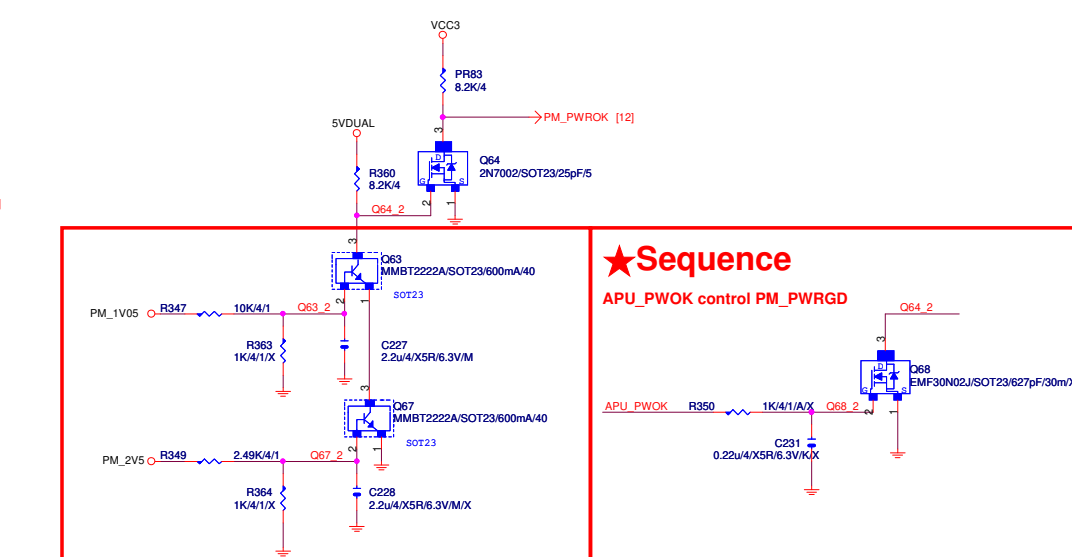
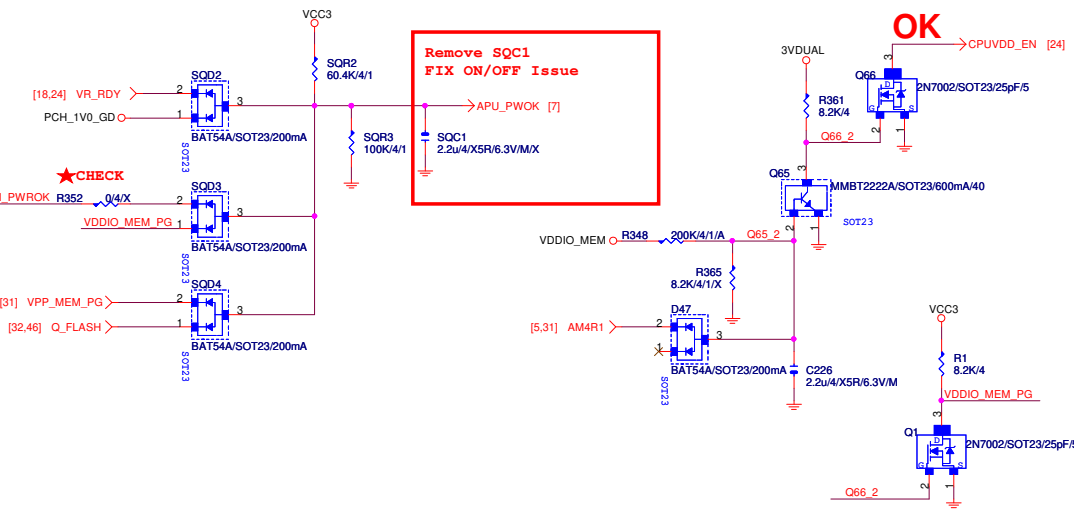
Hardware Monitor circuits - VOLTAGE

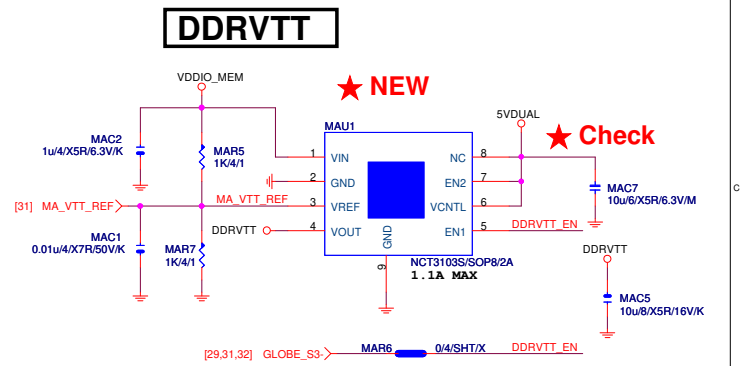
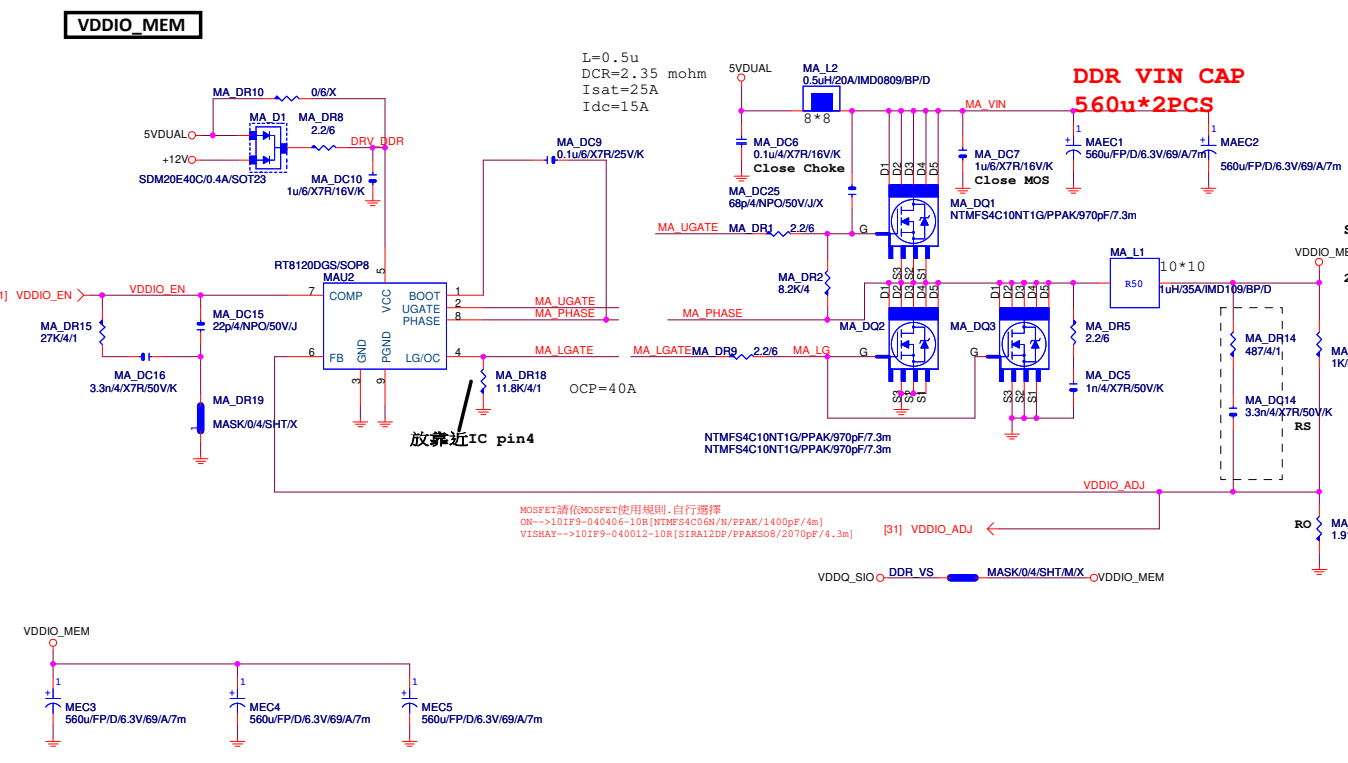
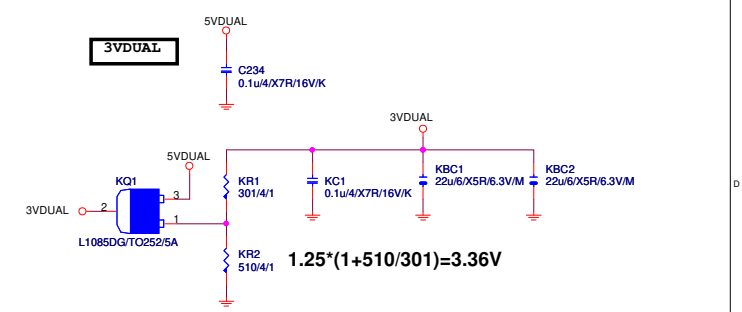
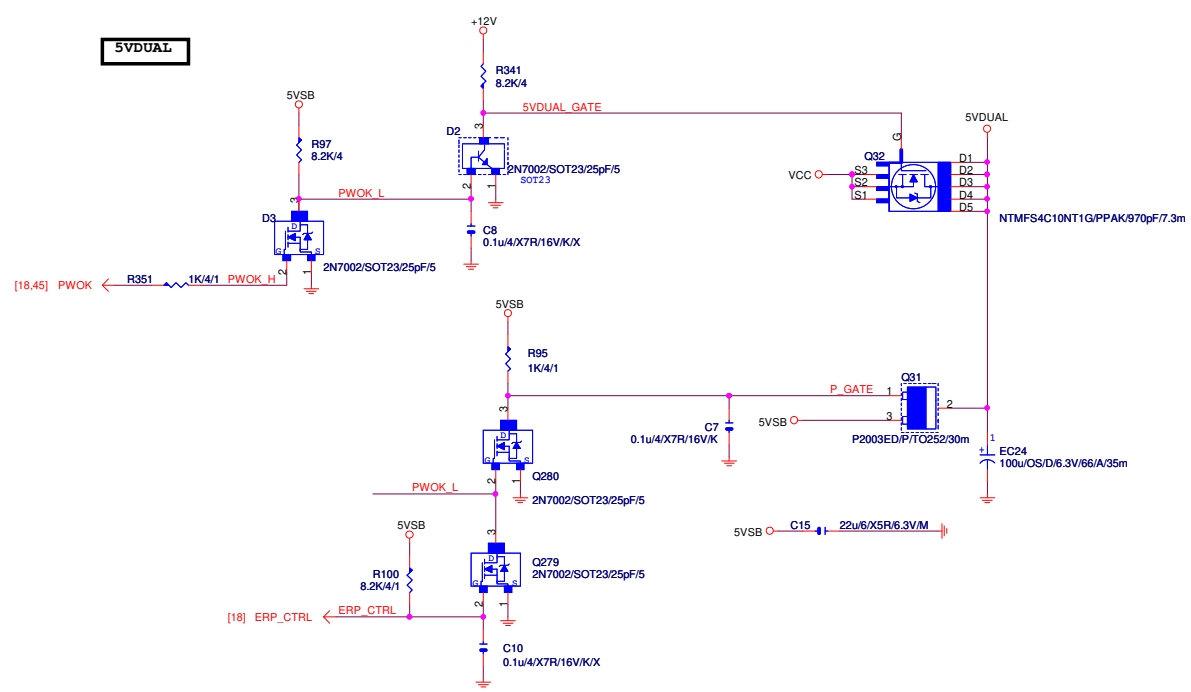


★Update 2015.04.22 remove.

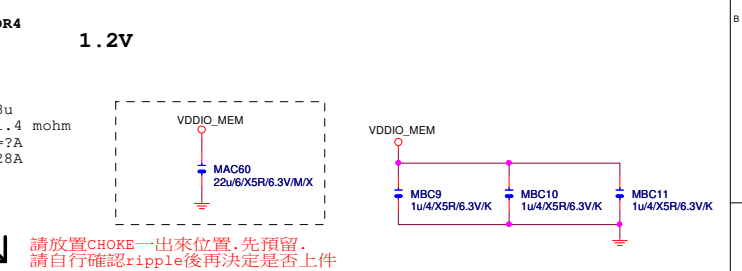
REV:0.1



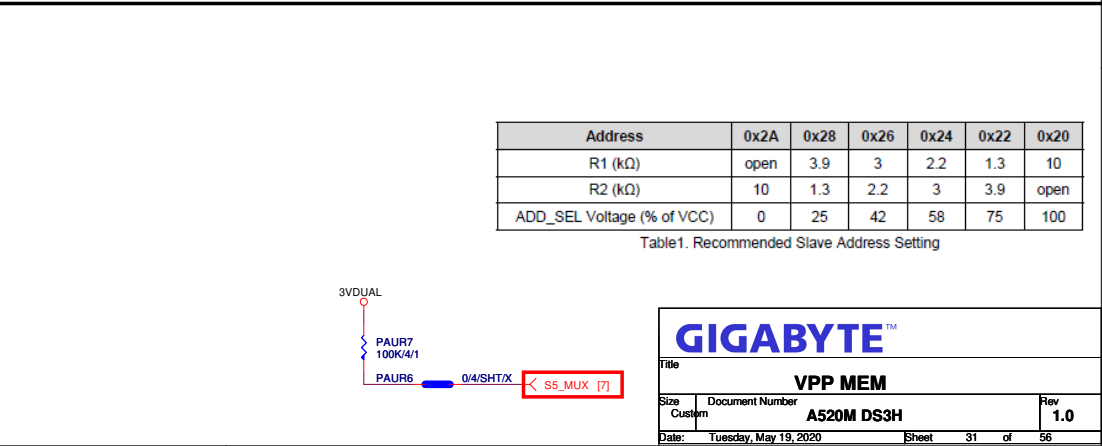
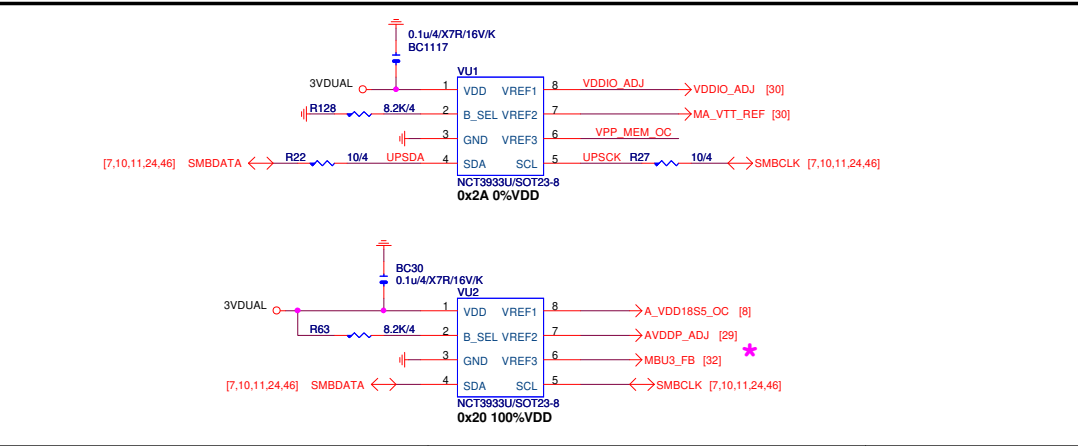
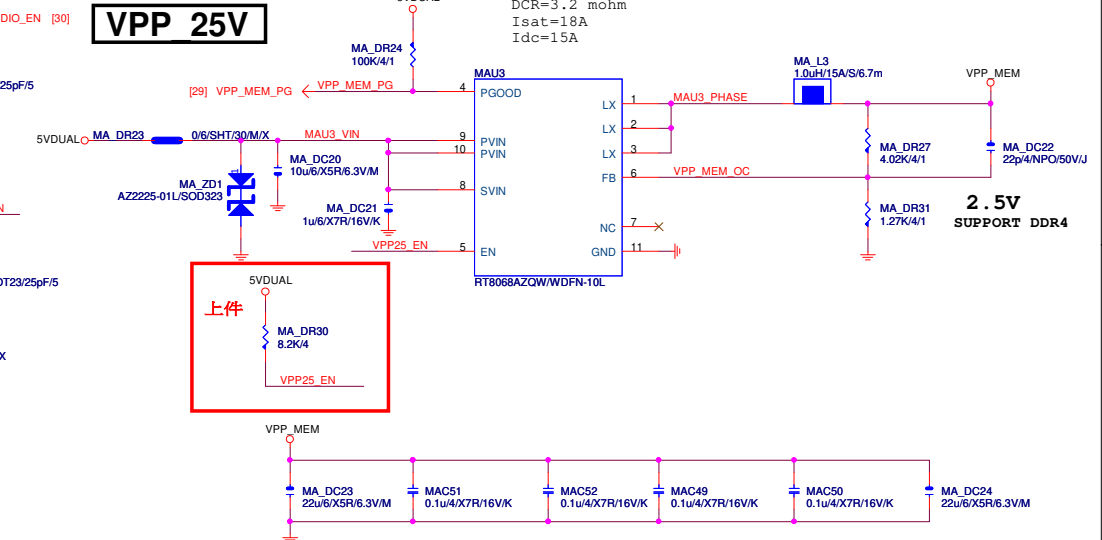
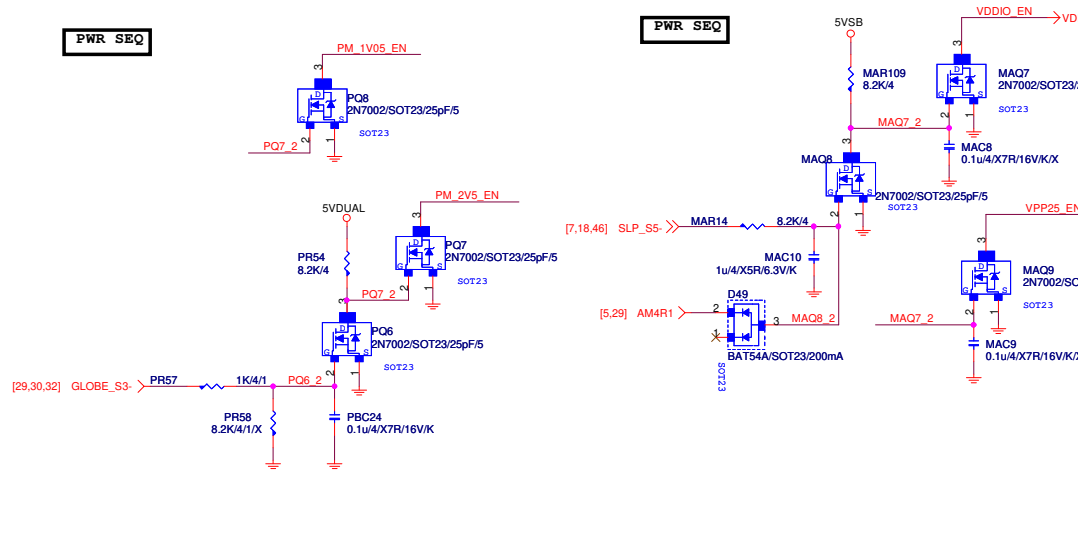
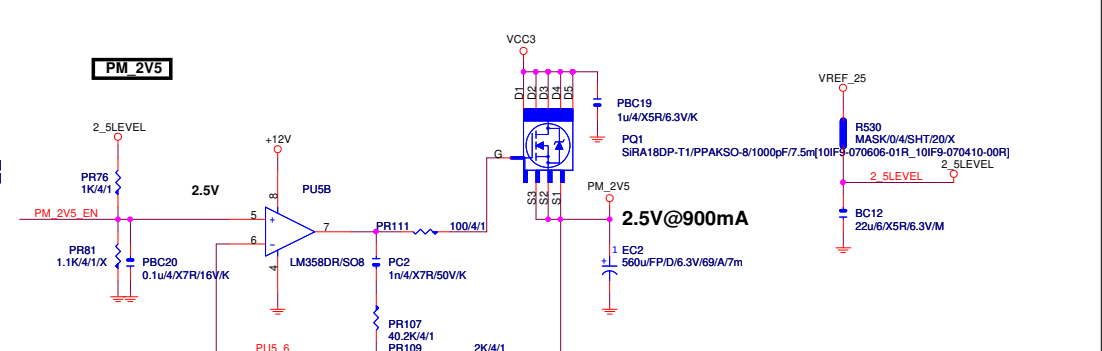
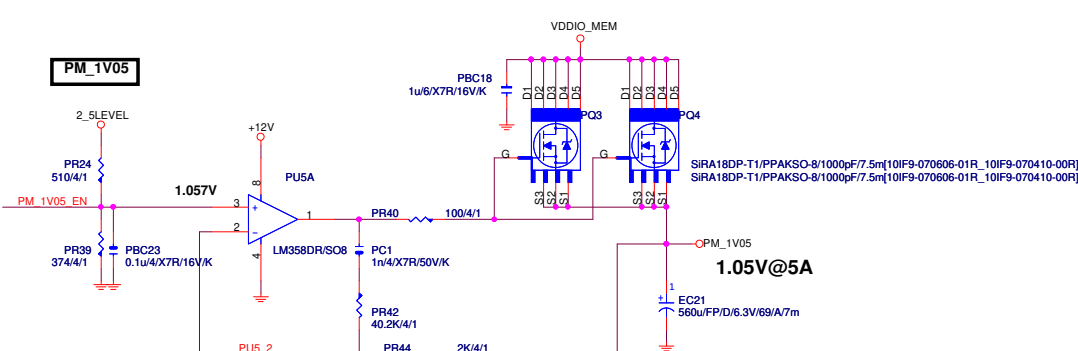




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Remote sense請從最重的負載端點拉回



Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

Table1. Recommended Slave Address Setting

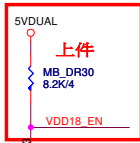
GIGABYTE

Title: **VPP MEM**

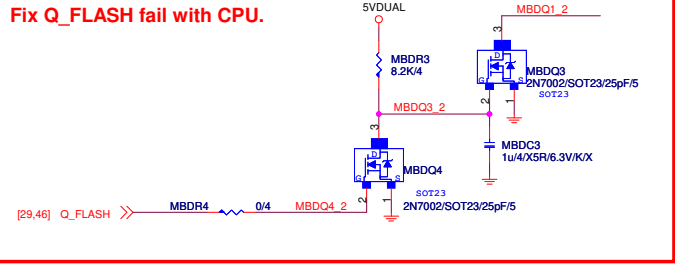
Size: Custom Document Number: **A520M DS3H** Rev: **1.0**

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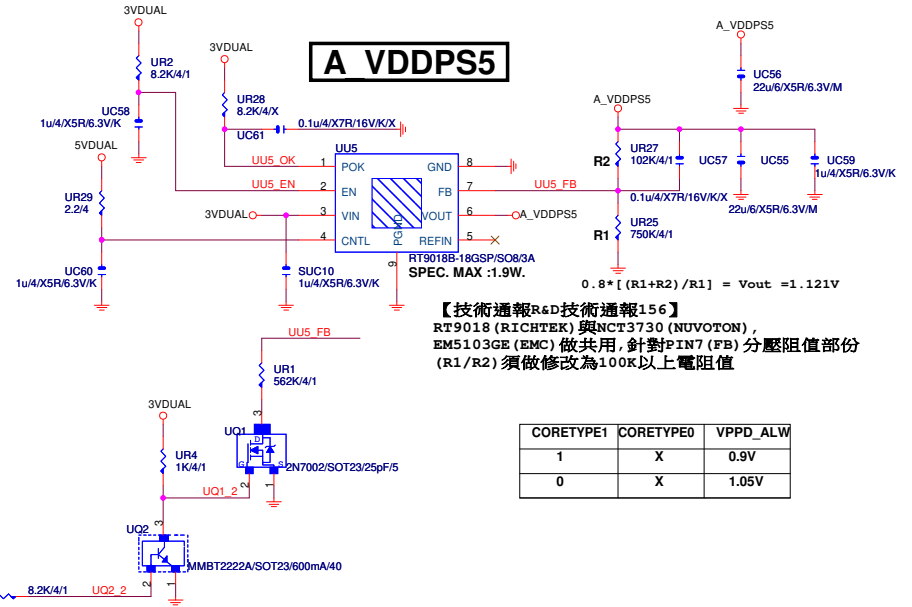
PWR_SEQ



Fix Q_FLASH fail with CPU.



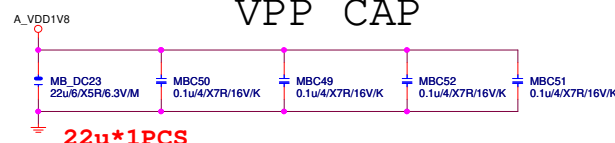
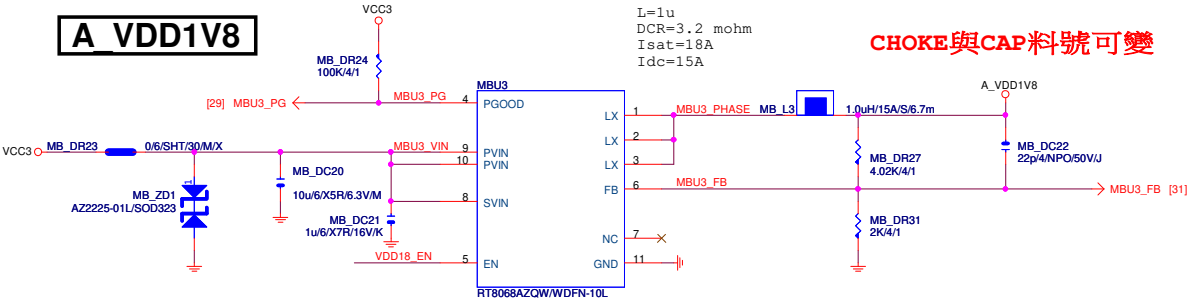
A VDDPS5



CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

REV:0.4

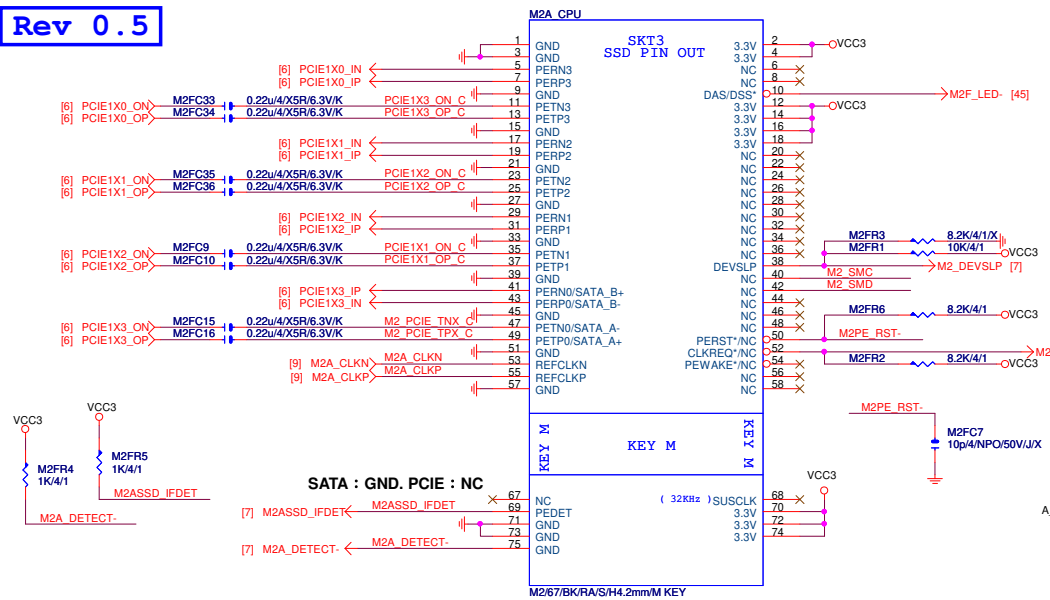
A VDD1V8



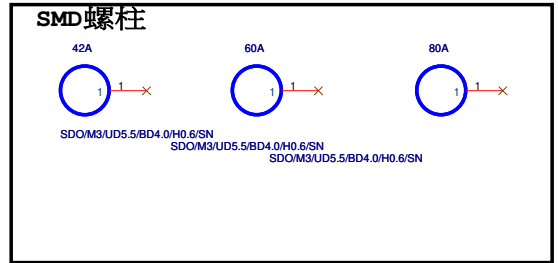
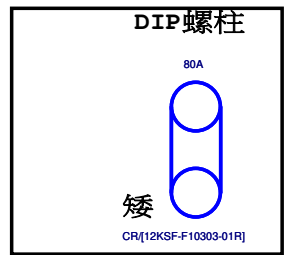
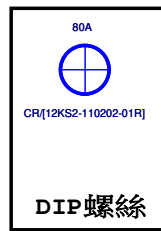
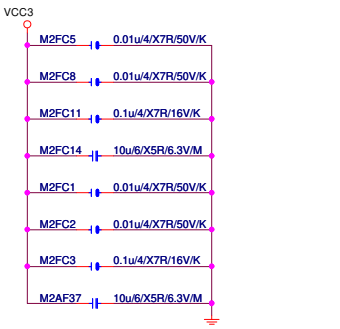
GIGABYTE™

Title		
FAN, A_VDD1V8		
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Rev 0.5



Footprint : NGFF-M-75P-8CM-09MM-SMD



Rev: 0.2

請選擇適用的USBport :
SOC/UD7/UD5/G1/G7 : USB4
;UD3/G5:USB6

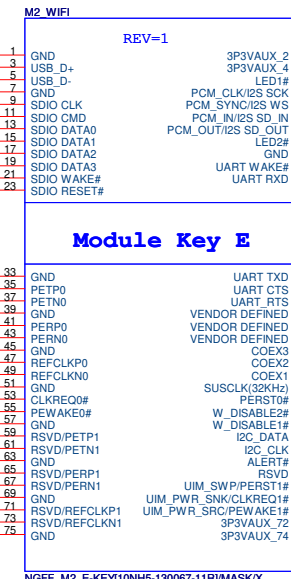
PCIE:15/4/4/15(breakout min 8/4/4/8)
外層Impedance=85 +/- 17.5%

PCIE:15/4/4/15(breakout min 8/4/4/8)
內層 Impedance=85 +/- 12%

WIFI use PCIE port4 in X99

NET 可變

WIFI_CLKREQ connect to relative pin.



M2 WIFI SLOT MASK

Footprint Notice.

★Update 2015-07-22
★Footprint for
直立式 SMD:
WIFI-EKEY

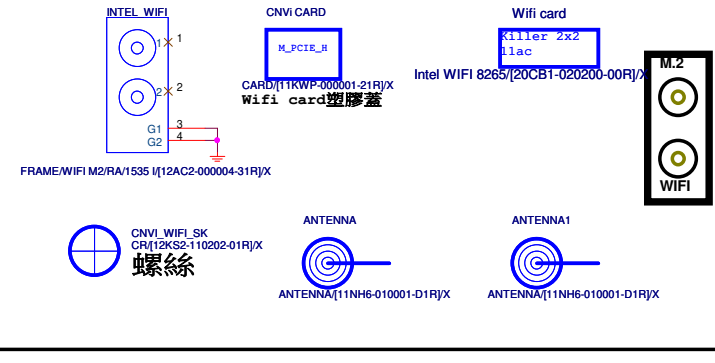
Footprint Notice.

★Update 2015-07-22
★Footprint for
橫躺式 SMD: NGFF-E-75P-2

FOR M.2 WIFI MODULE @ REAR PANEL

★Update 2015-02-11

一套WIFI MODULE包含外框+WIFI CARD+天線



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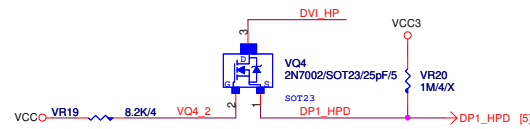
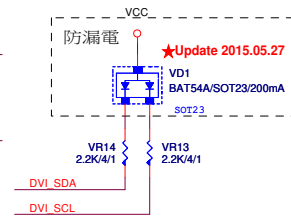
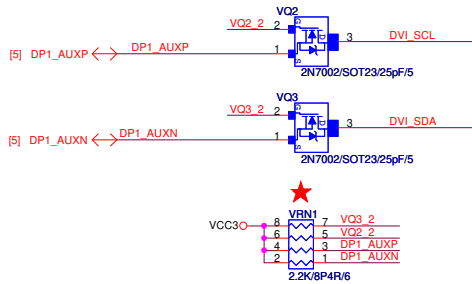
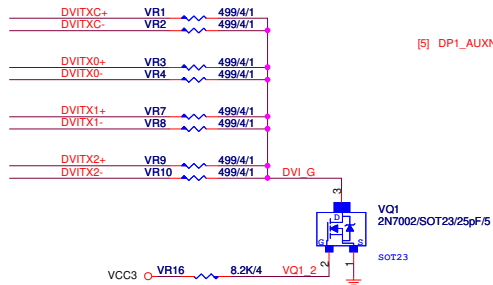
M.2 SOCKET

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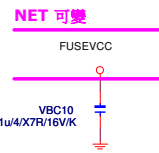
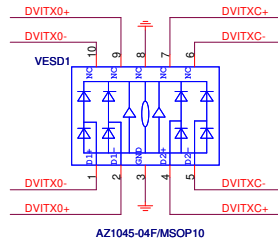
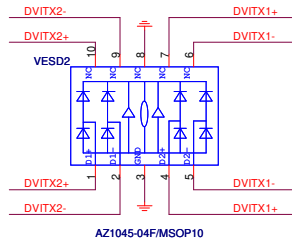
Rev: 0.73

DVI CONN

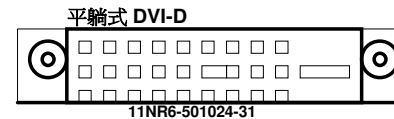
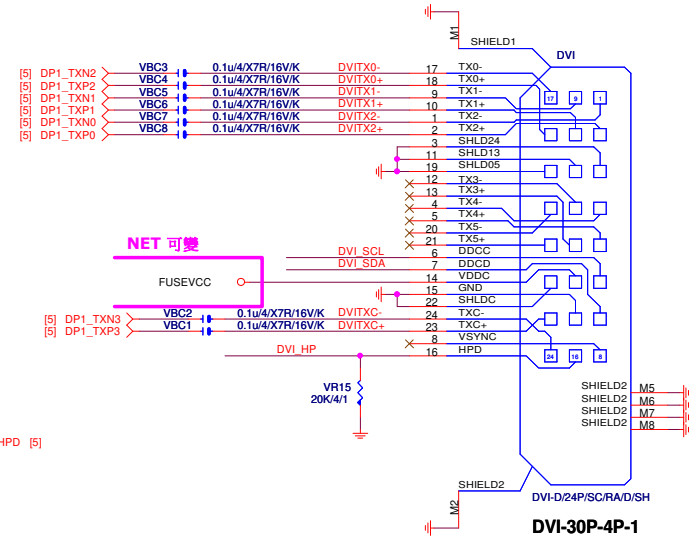
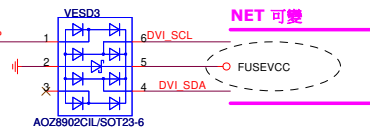
DVI: 20/4/6/4/20
Impedance=85 +- 17.5%



Close to connector

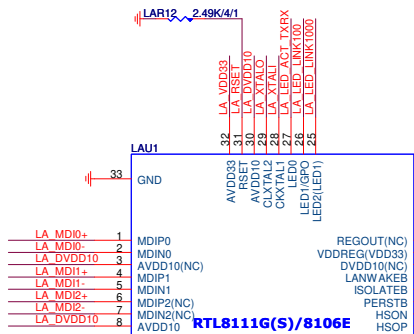


Close to connector



GIGABYTE™		
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KB_USB_DEC PWR		
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Custom		
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1.0		

LAN:RTL8111G R2.03

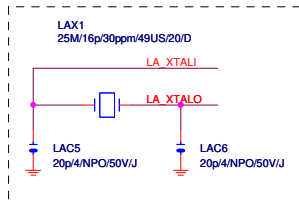


SRCCCLK-->50歐姆: [18/4/10/4/18]

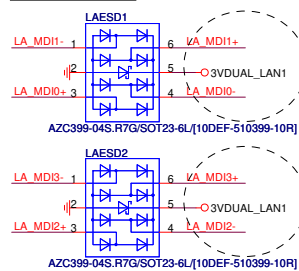
L1+CLK REQ# 節能:
需對應LA_SRCCLK_LAN之CLKREQ#

離IC近越好

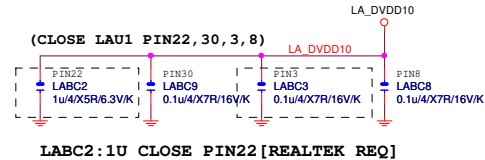
LA_ML-->80歐姆: [15/5/5/5/15]



MDI ESD

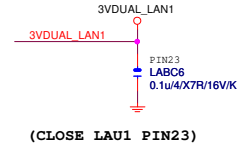


LAN POWER

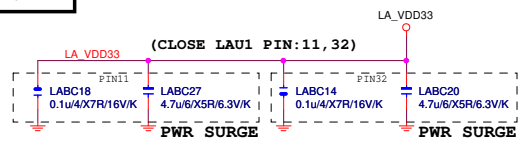


LAN POWER

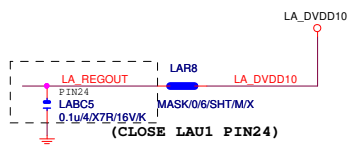
note: lan power連接及電流



LAN POWER



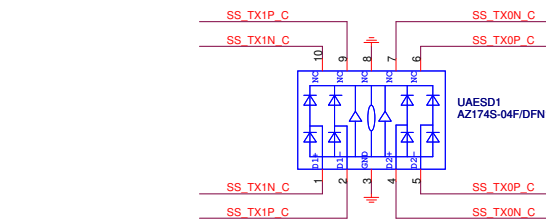
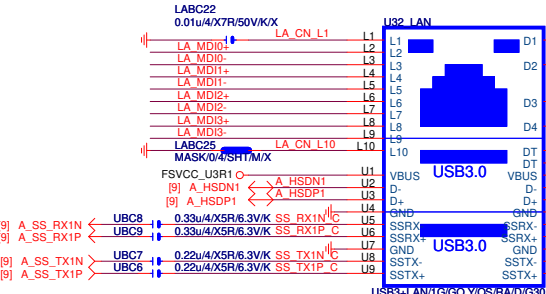
LAN POWER



USB_LAN CONNECTOR R2.03

USB_LAN CONNECTOR

[RTL8111G]



USB3.0

USB3.0

USB3.0

USB3.0

USB3.0

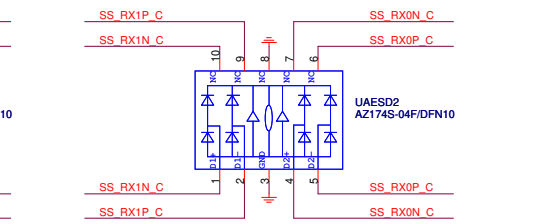
USB3.0

USB3.0

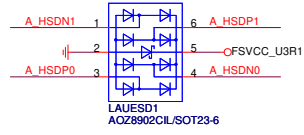
USB3.0

USB3.0

CPU SIDE



RMA ESD PROTECT



USB POWER



Close to connector
USB_LAN 2-Port 2.0A
FUSE-0805

EMI

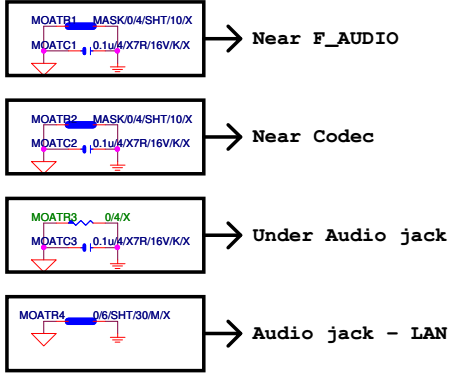
LAN AGND change GND
Remove Short Pad

LAN POWER



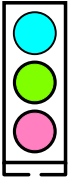
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*量産前, 0ohm改short pad

AZALIA JACK

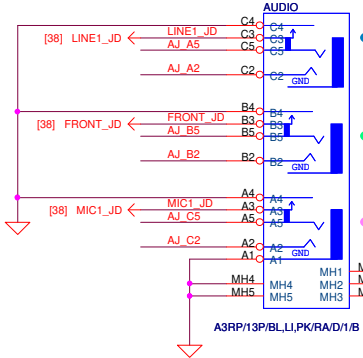


AZALIA JACK

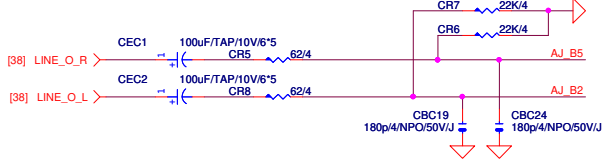
BLUE
LINE-IN

GREEN
LINE-OUT

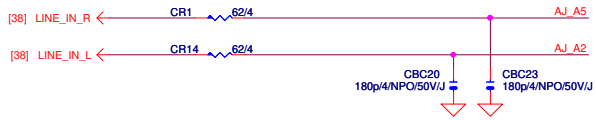
PINK
MIC-IN



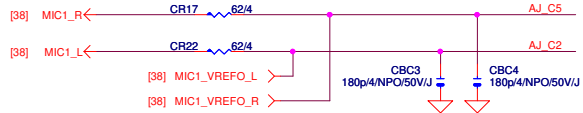
LINE-OUT



LINE-IN



MIC-IN

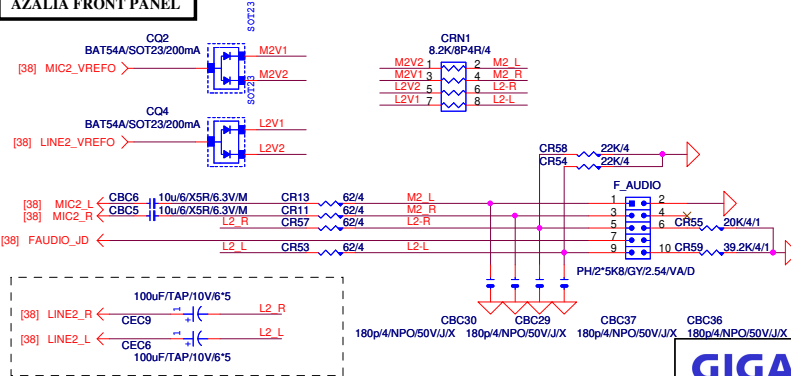


SURROUND

CEN/LFE

SURR BACK

AZALIA FRONT PANEL



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Title
AUDIO JACK

Size Custom Document Number
A520M DS3H

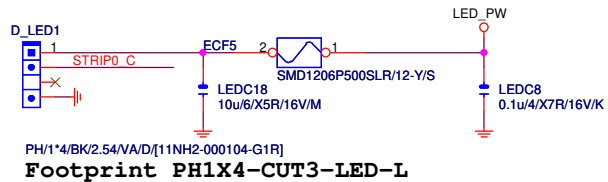
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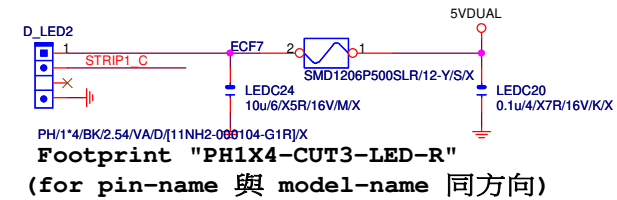
第六區 LED (靠近左上板邊位置)

Digital LED Strip1

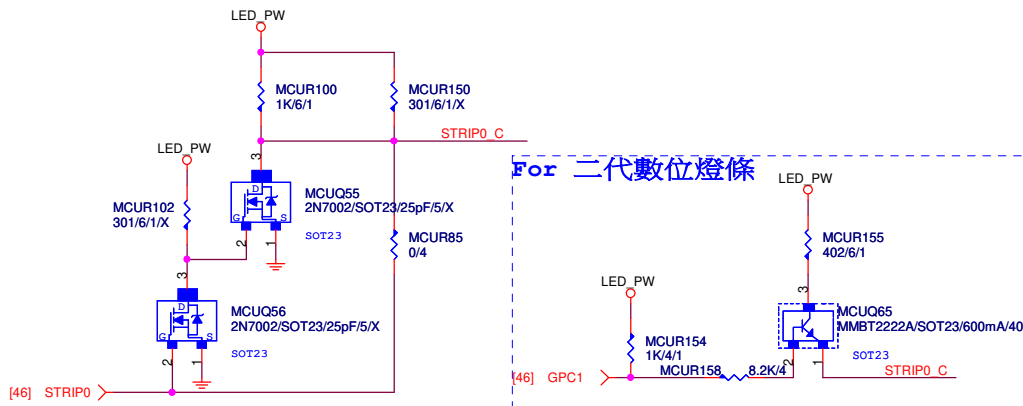


第七區 (靠近右下CPU板邊位置)

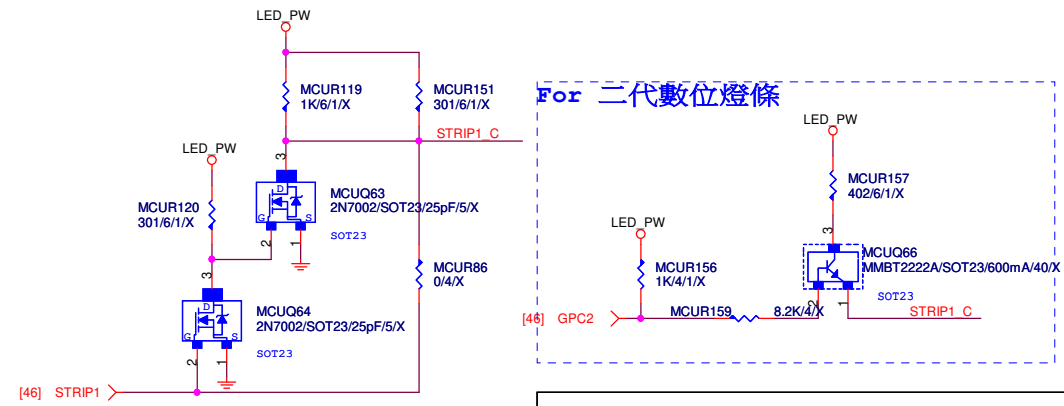
Digital LED Strip2



燈條 Level shift

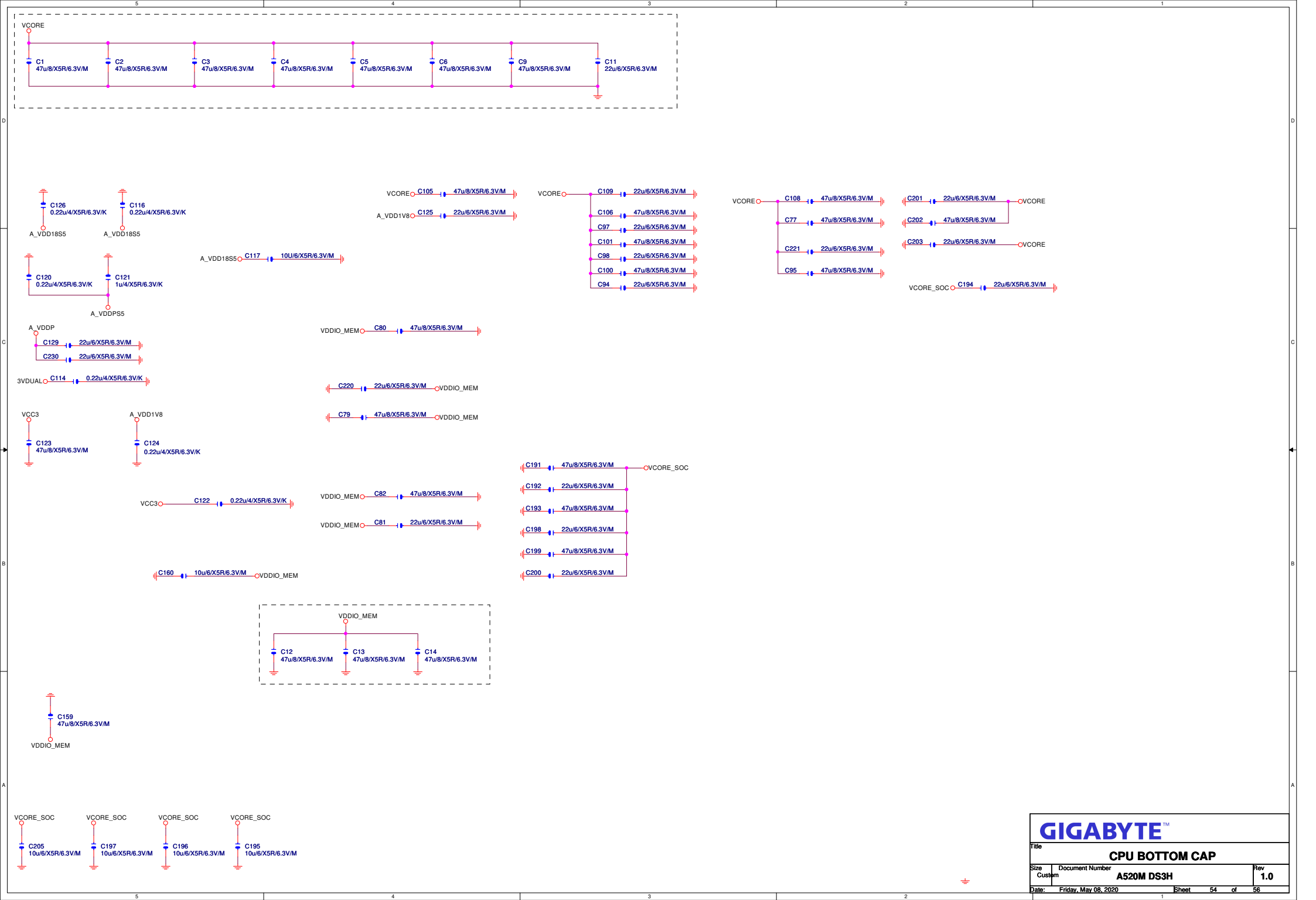


燈條 Level shift A520M DS3H [NA]

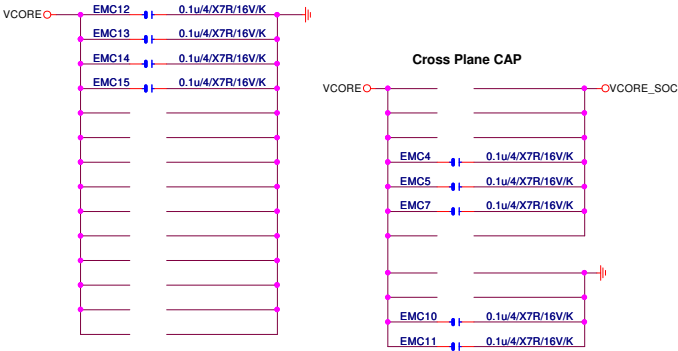
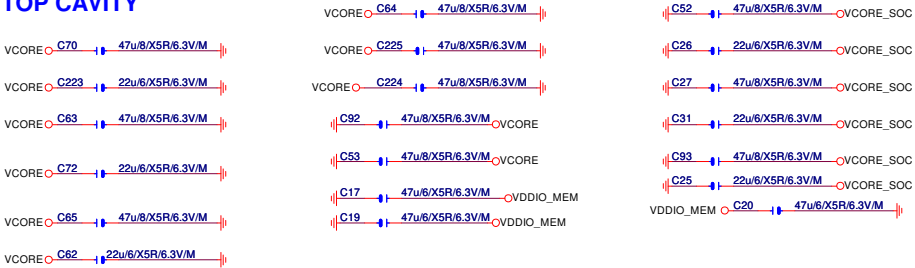


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D_LED		
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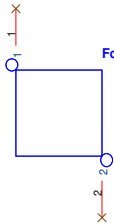


CPU TOP CAVITY



(A520M DS3H使用)

PCH_HS



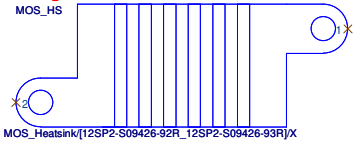
Footprint : BGAHSINK_SB-N
PM_HS1
PM_HS([12SP2-030005-51R_12SP2-030005-52R_12SP2-030005-53R_12SP2-030005-54R])

(同B450M S2H)

(A520M AORUS ELITE 使用)

MOS_HS

Footprint: MOSHSINK-SNIPERB8-T



(A520M AORUS ELITE 使用)

PCH_HS

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